JEDEC STANDARD

Compression Attached Memory Module (CAMM2) Common Standard

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COMPRESSION ATTACHED MEMORY MODULE (CAMM2) COMMON STANDARD

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COMPRESSION ATTACHED MEMORY MODULE (CAMM2) COMMON STANDARD

(From JEDEC Board Ballot JCB-25-73, formulated under the cognizance of the JC-45 committee on DRAM Modules, item 2290.07F).

1 Scope

This standard defines the electrical and mechanical requirements for Double Data Rate, Synchronous DRAM Compression-Attached Memory Modules (DDR5 SDRAM CAMM2s) and Low Power Double Data Rate, Synchronous DRAM Compression-Attached Memory Modules (LP5 SDRAM CAMM2s). These DDR5 and LP5 CAMM2s are intended for use as main memory when installed in computers, laptops, and other systems.

“CAMM” is general language to describe the module category. CAMM2 is the JEDEC standard version while prior CAMMs have been proprietary. In this document, “LP5” refers to either LPDDR5 or LPDDR5X DRAM.

Reference design examples are included which provide an initial basis for CAMM2 designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC5-6400, and beyond. CAMM2 with LPDDR5 DRAM is expected to start at 6400 MTs and increment upward in cadence with the DRAM speed capabilities. All CAMM2 implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Related standards:

- JESD79-5: DDR5 SDRAM
- JESD209-5: Low Power Double Data Rate (LPDDR) 5/5X
- JESD300-5: SPD5118 Hub and Serial Presence Detect Device Standard
- JESD301-2: PMIC5100 Power Management IC Standard
- JESD301-3: PMIC5200 Power Management IC Standard
- JESD400-5: DDR5 Serial Presence Detect (SPD) Contents
- JESD406-5: LPDDR5/5X Serial Presence Detect (SPD) Contents
- JESD401-5: DDR5 DIMM Labels
- JESD403-1: JEDEC Module Sideband Bus (SidebandBus)
- MO-210: Plastic Bottom Grid Array, 0.80 mm Pitch, Rectangular Family Package
- MO-338: 315-ball, pattern A CAMM2 Package

1 Scope (cont'd)

Table 1 — Product Family Attributes

Module Organization	DDR x64 (x32, 2 subchannels) = Single Channel CAMM2 DDR x72 ECC (x36, 2 subchannels) = Single Channel CAMM2 DDR x128(x32, 4 subchannels) = Dual Channel CAMM2 DDR x144 ECC (x36, 4 subchannels) = Dual Channel CAMM2 LPDDR x128 (x16, 8 subchannels)	
Module Dimensions (nominal)	Various form factors with X = 78 mm, Y = 29.6to 68 mm	MO-357 MO-358
Pin Count and Pitch	Variation AXXX for dual-channel CAMM2: 356 pins on 1.0 x 1.38 mm centers with ground shields interposed between rows Variation BXXX for single-channel CAMM2s: 178 pins on 1.0 x 1.38 mm centers with ground shields interposed between rows Variation CXXX for dual-channel CAMM2s: 644 pins on 1.0 x 1.38 mm centers with no ground shields: Variation DXXX for dual-channel CAMM2s: 666 pins on 1.0 x 1.38 mm centers with no ground shields:	SO-032
DDR5 SDRAMs Supported	16 Gb, 24 Gb, 32 Gb	MO-210
LP5 SDRAMs supported	32 Gb (2x16), 64 Gb(4x16), 128 Gb (8x8)	
Capacity	8 GB - 128 GB	
SDRAM width	X8 DDR5, x16 DDR5, x32 LP5	
Serial Presence Detect with Thermal Sensor	1024 byte	JESD300-5
PMIC	PMIC5100 for DDR5 PMIC5200 for LP5	JESD301-2 – DDR5 JESD301-3 for LP5
Input voltage	5V (VIN_BULK)	JESD301-2 – DDR5 JESD301-3 for LP5
Interface	1.1 V signaling for DDR5 0.5 V DQ/DQS/WCK (differential) signaling for LP5 1.05 V Addr/Clock(differential) signaling for LP5	

2 Environmental Requirements

CAMM2s are intended for use in these environments:

- Mobile computing environments that have limited capacity for heat dissipation.
- Standard office environments for desktop and AIO systems that have heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	
TOPR	DDR5 DRAM Operating Temperature	0 to +85 0 to +95	°C	1x Refresh 2x Refresh
TOPR	LP5 DRAM Operating Temperature	0 to +85	°C	Per JESD209-5 Table 400
TSTG	Storage Temperature	-55 to +100	°C	

NOTES:

1. Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs is at the minimum and maximum values. See JESD402-1 for details.
2. Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

3 Connector Pinouts and Signal Descriptions

3.1 Power, Ground, and Sideband Signal Descriptions

Table 3 — Power, Ground, and Sideband Signal Descriptions

Signal	Type	I/O Level	Function
ALERT_n	Input/ Output	VDDQ	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Use of this signal is system dependent. Pull up pin to VDDQ.
HSA	Input	2.1 V max	Host Sideband Bus device ID address pin: input to a Hub or other client device to distinguish between identical devices in the I3C-Basic/I2C address range.
HSCL	Input	1.0 V – 3.3V	Host Sideband Bus clock, supplied by the controller. Refer to JESD300-5 and JESD403-1
HSDA	Input/ Output	1.0 V – 3.3V	Host Sideband Bus data, connected from the controller to Hub or Host bus Target devices. Refer to JESD300-5 and JESD403-1
PWR_EN	Input	1.8 V or 3.3 V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin. Recommended pullup to 1.8 V. PMIC is 3.3 V tolerant.
PWR_GOOD	Input/ Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.

Table 3 — Power, Ground, and Sideband Signal Descriptions (cont'd)

Signal	Type	I/O Level	Function
RESET_n	Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
RFU	NA	NA	Reserved for Future Use. Circular pads are required within the CAMM2 footprint to assure future RFU pins are not shorted to ground. See MO-357 and MO-358 for pad sizes and placement. No electrical connection is present on CAMM2. Motherboards must pull down these RFU's to assure no unintended effects of floating pins.
RFU DDR6	NA	NA	Reserved for Future Use. These locations are not populated with pins in the current CAMM2 connector but are intentionally spaced at 1 x 1.14 mm such that a future standard could add contacts at these locations.
UNLOCK	Input	1.8 V	If PMIC supports UNLOCK, then when this pin is high upon assertion of VR_EN, the PMIC register bit 0x2F[2] is set high and follows the UNLOCK pin state. When this pin is low upon assertion of VR_EN, then 0x2F[2] is set low and the PMIC enters regulation with registers locked. 220K ohm pulldown'n' to ground on module at PMIC input is required to default to secure state. 22K ohm pull up on motherboards is recommended to indicate support for UNLOCK at VR_EN assertion. Support is optional but highly recommended for new designs that can drive UNLOCK from a secure GPIO source.
VIN_BULK	Supply	4.25 - 5.5 V	5 V (nom) power input supply to the PMIC for analog circuits.

NOTES:

1. Sideband signals may be represented with signal suffix _0 or _1 to indicate channel number. CAMM2 designs must use the sideband signals with _0 suffix. The use of _0 and _1 suffix occurs on motherboard designs that support mechanical stacking of single-channel CAMM2

3.2 DDR5 Signal Descriptions

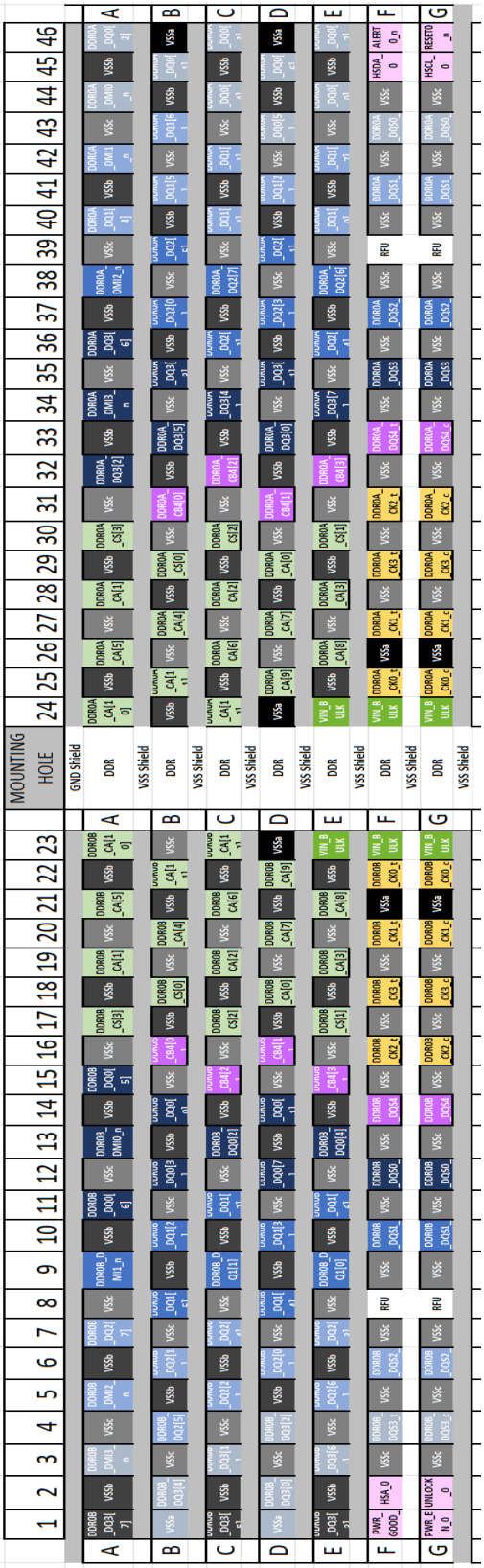
Table 4 — DDR5 Signal Descriptions

Signal	Type	I/O Level	Function
CK[3:0]_t CK[3:0]_c	Input	VDDQ	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled when crossing the positive edge of CK_t and negative edge of CK_c.
CA[12:0]	Input	VDDQ	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS[3:0]_n	Input	VDDQ	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks.
DQ[31:0]	Input/ Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst.
CB[3:0]	Input/ Output	VDDQ	DIMM ECC check bits
DQS[4:0]_t DQS[4:0]_c	Input/ Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended. (DQS[4] is for ECC)
DMI[3:0]_n	Input	VDDQ	Data Mask Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.

NOTES:

- Subchannel groups are represented with signal prefixes DDR0A_, DDR0B_, DDR1A_, and DDR1B_. All the above signals are duplicated for each subchannel.
- Informative: In other documents, CK naming uses a convention of CK[1:0]_[1:0][B:A]_t/c for A and B Channels and two Channels [1:0]. The naming conversions are:
  - DDR0A_CK0_t = CK0_0A_t and DDR0A_CK0_c = CK0_0A_c
  - DDR0B_CK1_t = CK0_0B_t and DDR0B_CK1_c = CK0_0B_c
  - DDR1A_CK0_t = CK1_0A_t and DDR1A_CK2_c = CK1_0A_c
  - DDR1B_CK1_t = CK1_0B_t and DDR1B_CK3_c = CK1_0B_c

3.3 DDR5 Single-Channel CAMM2 Connector Pin Assignments



3.4 DDR5 Single-Channel Pinout Table

Table 5 — DDR5 Single-Channel CAMM2 Connector Pin Wiring Assignments

SIGNAL NAME	PIN NUMBER
ALERT0_n	F46
DDR0A_CA[0]	D29
DDR0A_CA[1]	A28
DDR0A_CA[10]	A24
DDR0A_CA[11]	B25
DDR0A_CA[12]	C24
DDR0A_CA[2]	C28
DDR0A_CA[3]	E28
DDR0A_CA[4]	B27
DDR0A_CA[5]	A26
DDR0A_CA[6]	C26
DDR0A_CA[7]	D27
DDR0A_CA[8]	E26
DDR0A_CA[9]	D25
DDR0A_CB4[0]	B31
DDR0A_CB4[1]	D31
DDR0A_CB4[2]	C32
DDR0A_CB4[3]	E32
DDR0A_CK0_c	G25
DDR0A_CK0_t	F25
DDR0A_CK1_c	G27
DDR0A_CK1_t	F27
DDR0A_CK2_c	G31
DDR0A_CK2_t	F31
DDR0A_CK3_c	G29
DDR0A_CK3_t	F29
DDR0A_CS[0]	B29
DDR0A_CS[1]	E30
DDR0A_CS[2]	C30
DDR0A_CS[3]	A30
DDR0A_DMI0_n	A44
DDR0A_DMI1_n	A42
DDR0A_DMI2_n	A38
DDR0A_DMI3_n	A34
DDR0A_DQ0[0]	E44
DDR0A_DQ0[1]	B45
DDR0A_DQ0[2]	A46
DDR0A_DQ0[3]	C46
DDR0A_DQ0[4]	C44
DDR0A_DQ0[5]	D43
DDR0A_DQ0[6]	D45
DDR0A_DQ0[7]	E46
DDR0A_DQ1[0]	E40

SIGNAL NAME	PIN NUMBER
DDR0B_CA[0]	D18
DDR0B_CA[1]	A19
DDR0B_CA[10]	A23
DDR0B_CA[11]	B22
DDR0B_CA[12]	C23
DDR0B_CA[2]	C19
DDR0B_CA[3]	E19
DDR0B_CA[4]	B20
DDR0B_CA[5]	A21
DDR0B_CA[6]	C21
DDR0B_CA[7]	D20
DDR0B_CA[8]	E21
DDR0B_CA[9]	D22
DDR0B_CB4[0]	B16
DDR0B_CB4[1]	D16
DDR0B_CB4[2]	C15
DDR0B_CB4[3]	E15
DDR0B_CK0_c	G22
DDR0B_CK0_t	F22
DDR0B_CK1_c	G20
DDR0B_CK1_t	F20
DDR0B_CK2_c	G16
DDR0B_CK2_t	F16
DDR0B_CK3_c	G18
DDR0B_CK3_t	F18
DDR0B_CS[0]	B18
DDR0B_CS[1]	E17
DDR0B_CS[2]	C17
DDR0B_CS[3]	A17
DDR0B_DMI0_n	A13
DDR0B_DMI1_n	A09
DDR0B_DMI2_n	A05
DDR0B_DMI3_n	A03
DDR0B_DQ0[0]	B14
DDR0B_DQ0[1]	D14
DDR0B_DQ0[2]	C13
DDR0B_DQ0[3]	B12
DDR0B_DQ0[4]	E13
DDR0B_DQ0[5]	A15
DDR0B_DQ0[6]	A11
DDR0B_DQ0[7]	D12
DDR0B_DQ1[0]	E09

Table 5 — DDR5 Single-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

`	PIN NUMBER
DDR0A_DQ1[1]	C42
DDR0A_DQ1[2]	D41
DDR0A_DQ1[3]	C40
DDR0A_DQ1[4]	A40
DDR0A_DQ1[5]	B41
DDR0A_DQ1[6]	B43
DDR0A_DQ1[7]	E42
DDR0A_DQ2[0]	B37
DDR0A_DQ2[1]	D39
DDR0A_DQ2[2]	C36
DDR0A_DQ2[3]	D37
DDR0A_DQ2[4]	E36
DDR0A_DQ2[5]	B39
DDR0A_DQ2[6]	E38
DDR0A_DQ2[7]	C38
DDR0A_DQ3[0]	D33
DDR0A_DQ3[1]	D35
DDR0A_DQ3[2]	A32
DDR0A_DQ3[3]	B35
DDR0A_DQ3[4]	C34
DDR0A_DQ3[5]	B33
DDR0A_DQ3[6]	A36
DDR0A_DQ3[7]	E34
DDR0A_DQS0_c	G43
DDR0A_DQS0_t	F43
DDR0A_DQS1_c	G41
DDR0A_DQS1_t	F41
DDR0A_DQS2_c	G37
DDR0A_DQS2_t	F37
DDR0A_DQS3_c	G35
DDR0A_DQS3_t	F35
DDR0A_DQS4_c	G33
DDR0A_DQS4_t	F33

SIGNAL NAME	PIN NUMBER
DDR0B_DQ1[1]	C09
DDR0B_DQ1[2]	B10
DDR0B_DQ1[3]	D10
DDR0B_DQ1[4]	D08
DDR0B_DQ1[5]	B08
DDR0B_DQ1[6]	E11
DDR0B_DQ1[7]	C11
DDR0B_DQ2[0]	D06
DDR0B_DQ2[1]	B06
DDR0B_DQ2[2]	C05
DDR0B_DQ2[3]	E07
DDR0B_DQ2[4]	C07
DDR0B_DQ2[5]	B04
DDR0B_DQ2[6]	E05
DDR0B_DQ2[7]	A07
DDR0B_DQ3[0]	D02
DDR0B_DQ3[1]	C03
DDR0B_DQ3[2]	D04
DDR0B_DQ3[3]	E01
DDR0B_DQ3[4]	B02
DDR0B_DQ3[5]	C01
DDR0B_DQ3[6]	E03
DDR0B_DQ3[7]	A01
DDR0B_DQS0_c	G12
DDR0B_DQS0_t	F12
DDR0B_DQS1_c	G10
DDR0B_DQS1_t	F10
DDR0B_DQS2_c	G06
DDR0B_DQS2_t	F06
DDR0B_DQS3_c	G04
DDR0B_DQS3_t	F04
DDR0B_DQS4_c	G14
DDR0B_DQS4_t	F14
HSA_0	F02
HSCL_0	G45
HSDA_0	F45
PWR_EN_0	G01
PWR_GOOD_0	F01
RESET0_n	G46
UNLOCK_0	G02

Table 5 — DDR5 Single-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

SIGNAL NAME	PIN NUMBER
RFU	F08, F39, G08, G39
VIN_BULK	E23, E24, F23, F24, G23, G24
VSSa	B01, B46, D01, D23, D24, D46, F21, F26, G21, G26
VSSb	A02, A06, A10, A14, A18, A22, A25, A29, A33, A37, A41, A45, B05, B09, B13, B17, B21, B24, B28, B32, B36, B40, B44, C02, C06, C10, C14, C18, C22, C25, C29, C33, C37, C41, C45, D05, D09, D13, D17, D21, D28, D32, D36, D40, D44, E02, E06, E10, E14, E18, E22, E25, E29, E33, E37, E41, E45
VSSc	A04, A08, A12, A16, A20, A27, A31, A35, A39, A43, B03, B07, B11, B15, B19, B23, B26, B30, B34, B38, B42, C04, C08, C12, C16, C20, C27, C31, C35, C39, C43, D03, D07, D11, D15, D19, D26, D30, D34, D38, D42, E04, E08, E12, E16, E20, E27, E31, E35, E39, E43, F03, F05, F07, F09, F11, F13, F15, F17, F19, F28, F30, F32, F34, F36, F38, F40, F42, F44, G03, G05, G07, G09, G11, G13, G15, G17, G19, G28, G30, G32, G34, G36, G38, G40, G42, G44

NOTES:

1. VSSa are ground pins that are populated in this Variation BXXX of the CAMM2 connector.
2. VSSb and VSSc are ground pins that are populated in future variations of the CAMM2 Connector. They are intended to improve crosstalk performance of the CAMM2 connector. JEDEC JC-11 defines the ground pin population requirements based on connector performance requirements.

3.5 DDR5 Dual-Channel CAMM2 Connector Pin Assignments

3.6 DDR5 Dual-Channel Pinout Table

Table 6 — DDR5 Dual-Channel CAMM2 Connector Pin Wiring Assignments

SIGNAL NAME	PIN NUMBER
ALERT0_n	N46
ALERT1_n	F46
DDR0A_CA[0]	L29
DDR0A_CA[1]	H28
DDR0A_CA[10]	H24
DDR0A_CA[11]	J25
DDR0A_CA[12]	K24
DDR0A_CA[2]	K28
DDR0A_CA[3]	M28
DDR0A_CA[4]	J27
DDR0A_CA[5]	H26
DDR0A_CA[6]	K26
DDR0A_CA[7]	L27
DDR0A_CA[8]	M26
DDR0A_CA[9]	L25
DDR0A_CB4[0]	J31
DDR0A_CB4[1]	L31
DDR0A_CB4[2]	K32
DDR0A_CB4[3]	M32
DDR0A_CK0_c	P25
DDR0A_CK0_t	N25
DDR0A_CK1_c	P27
DDR0A_CK1_t	N27
DDR0A_CK2_c	P31
DDR0A_CK2_t	N31
DDR0A_CK3_c	P29
DDR0A_CK3_t	N29
DDR0A_CS[0]	J29
DDR0A_CS[1]	M30
DDR0A_CS[2]	K30
DDR0A_CS[3]	H30
DDR0A_DMI0_n	H44
DDR0A_DMI1_n	H42
DDR0A_DMI2_n	H38
DDR0A_DMI3_n	H34
DDR0A_DQ0[0]	M44
DDR0A_DQ0[1]	J45

SIGNAL NAME	PIN NUMBER
DDR1A_CA[0]	D29
DDR1A_CA[1]	A28
DDR1A_CA[10]	A24
DDR1A_CA[11]	B25
DDR1A_CA[12]	C24
DDR1A_CA[2]	C28
DDR1A_CA[3]	E28
DDR1A_CA[4]	B27
DDR1A_CA[5]	A26
DDR1A_CA[6]	C26
DDR1A_CA[7]	D27
DDR1A_CA[8]	E26
DDR1A_CA[9]	D25
DDR1A_CB4[0]	B31
DDR1A_CB4[1]	D31
DDR1A_CB4[2]	C32
DDR1A_CB4[3]	E32
DDR1A_CK0_c	G25
DDR1A_CK0_t	F25
DDR1A_CK1_c	G27
DDR1A_CK1_t	F27
DDR1A_CK2_c	G31
DDR1A_CK2_t	F31
DDR1A_CK3_c	G29
DDR1A_CK3_t	F29
DDR1A_CS[0]	B29
DDR1A_CS[1]	E30
DDR1A_CS[2]	C30
DDR1A_CS[3]	A30
DDR1A_DMI0_n	A44
DDR1A_DMI1_n	A42
DDR1A_DMI2_n	A38
DDR1A_DMI3_n	A34
DDR1A_DQ0[0]	E44
DDR1A_DQ0[1]	B45
DDR1A_DQ0[2]	A46
DDR1A_DQ0[3]	C46

Table 6 — DDR5 Dual-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

SIGNAL NAME	PIN NUMBER
DDR0A_DQ0[2]	H46
DDR0A_DQ0[3]	K46
DDR0A_DQ0[4]	K44
DDR0A_DQ0[5]	L43
DDR0A_DQ0[6]	L45
DDR0A_DQ0[7]	M46
DDR0A_DQ1[0]	M40
DDR0A_DQ1[1]	K42
DDR0A_DQ1[2]	L41
DDR0A_DQ1[3]	K40
DDR0A_DQ1[4]	H40
DDR0A_DQ1[5]	J41
DDR0A_DQ1[6]	J43
DDR0A_DQ1[7]	M42
DDR0A_DQ2[0]	J37
DDR0A_DQ2[1]	L39
DDR0A_DQ2[2]	K36
DDR0A_DQ2[3]	L37
DDR0A_DQ2[4]	M36
DDR0A_DQ2[5]	J39
DDR0A_DQ2[6]	M38
DDR0A_DQ2[7]	K38
DDR0A_DQ3[0]	L33
DDR0A_DQ3[1]	L35
DDR0A_DQ3[2]	H32
DDR0A_DQ3[3]	J35
DDR0A_DQ3[4]	K34
DDR0A_DQ3[5]	J33
DDR0A_DQ3[6]	H36
DDR0A_DQ3[7]	M34
DDR0A_DQS0_c	P43
DDR0A_DQS0_t	N43
DDR0A_DQS1_c	P41
DDR0A_DQS1_t	N41
DDR0A_DQS2_c	P37
DDR0A_DQS2_t	N37
DDR0A_DQS3_c	P35

SIGNAL NAME	PIN NUMBER
DDR1A_DQ0[4]	C44
DDR1A_DQ0[5]	D43
DDR1A_DQ0[6]	D45
DDR1A_DQ0[7]	E46
DDR1A_DQ1[0]	E40
DDR1A_DQ1[1]	C42
DDR1A_DQ1[2]	D41
DDR1A_DQ1[3]	C40
DDR1A_DQ1[4]	A40
DDR1A_DQ1[5]	B41
DDR1A_DQ1[6]	B43
DDR1A_DQ1[7]	E42
DDR1A_DQ2[0]	B37
DDR1A_DQ2[1]	D39
DDR1A_DQ2[2]	C36
DDR1A_DQ2[3]	D37
DDR1A_DQ2[4]	E36
DDR1A_DQ2[5]	B39
DDR1A_DQ2[6]	E38
DDR1A_DQ2[7]	C38
DDR1A_DQ3[0]	D33
DDR1A_DQ3[1]	D35
DDR1A_DQ3[2]	A32
DDR1A_DQ3[3]	B35
DDR1A_DQ3[4]	C34
DDR1A_DQ3[5]	B33
DDR1A_DQ3[6]	A36
DDR1A_DQ3[7]	E34
DDR1A_DQS0_c	G43
DDR1A_DQS0_t	F43
DDR1A_DQS1_c	G41
DDR1A_DQS1_t	F41
DDR1A_DQS2_c	G37
DDR1A_DQS2_t	F37
DDR1A_DQS3_c	G35
DDR1A_DQS3_t	F35
DDR1A_DQS4_c	G33

Table 6 — DDR5 Dual-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

SIGNAL NAME	PIN NUMBER
DDR0A_DQS3_t	N35
DDR0A_DQS4_c	P33
DDR0A_DQS4_t	N33
DDR0B_CA[0]	L18
DDR0B_CA[1]	H19
DDR0B_CA[10]	H23
DDR0B_CA[11]	J22
DDR0B_CA[12]	K23
DDR0B_CA[2]	K19
DDR0B_CA[3]	M19
DDR0B_CA[4]	J20
DDR0B_CA[5]	H21
DDR0B_CA[6]	K21
DDR0B_CA[7]	L20
DDR0B_CA[8]	M21
DDR0B_CA[9]	L22
DDR0B_CB4[0]	J16
DDR0B_CB4[1]	L16
DDR0B_CB4[2]	K15
DDR0B_CB4[3]	M15
DDR0B_CK0_c	P22
DDR0B_CK0_t	N22
DDR0B_CK1_c	P20
DDR0B_CK1_t	N20
DDR0B_CK2_c	P16
DDR0B_CK2_t	N16
DDR0B_CK3_c	P18
DDR0B_CK3_t	N18
DDR0B_CS[0]	J18
DDR0B_CS[1]	M17
DDR0B_CS[2]	K17
DDR0B_CS[3]	H17
DDR0B_DMI0_n	H13
DDR0B_DMI1_n	H09
DDR0B_DMI2_n	H05
DDR0B_DMI3_n	H03
DDR0B_DQ0[0]	J14
DDR0B_DQ0[1]	L14
DDR0B_DQ0[2]	K13
DDR0B_DQ0[3]	J12
DDR0B_DQ0[4]	M13

SIGNAL NAME	PIN NUMBER
DDR1A_DQS4_t	F33
DDR1B_CA[0]	D18
DDR1B_CA[1]	A19
DDR1B_CA[10]	A23
DDR1B_CA[11]	B22
DDR1B_CA[12]	C23
DDR1B_CA[2]	C19
DDR1B_CA[3]	E19
DDR1B_CA[4]	B20
DDR1B_CA[5]	A21
DDR1B_CA[6]	C21
DDR1B_CA[7]	D20
DDR1B_CA[8]	E21
DDR1B_CA[9]	D22
DDR1B_CB4[0]	B16
DDR1B_CB4[1]	D16
DDR1B_CB4[2]	C15
DDR1B_CB4[3]	E15
DDR1B_CK0_c	G22
DDR1B_CK0_t	F22
DDR1B_CK1_c	G20
DDR1B_CK1_t	F20
DDR1B_CK2_c	G16
DDR1B_CK2_t	F16
DDR1B_CK3_c	G18
DDR1B_CK3_t	F18
DDR1B_CS[0]	B18
DDR1B_CS[1]	E17
DDR1B_CS[2]	C17
DDR1B_CS[3]	A17
DDR1B_DMI0_n	A13
DDR1B_DMI1_n	A09
DDR1B_DMI2_n	A05
DDR1B_DMI3_n	A03
DDR1B_DQ0[0]	B14
DDR1B_DQ0[1]	D14
DDR1B_DQ0[2]	C13
DDR1B_DQ0[3]	B12
DDR1B_DQ0[4]	E13
DDR1B_DQ0[5]	A15
DDR1B_DQ0[6]	A11

Table 6 — DDR5 Dual-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

SIGNAL NAME	PIN NUMBER
DDR0B_DQ0[5]	H15
DDR0B_DQ0[6]	H11
DDR0B_DQ0[7]	L12
DDR0B_DQ1[0]	M09
DDR0B_DQ1[1]	K09
DDR0B_DQ1[2]	J10
DDR0B_DQ1[3]	L10
DDR0B_DQ1[4]	L08
DDR0B_DQ1[5]	J08
DDR0B_DQ1[6]	M11
DDR0B_DQ1[7]	K11
DDR0B_DQ2[0]	L06
DDR0B_DQ2[1]	J06
DDR0B_DQ2[2]	K05
DDR0B_DQ2[3]	M07
DDR0B_DQ2[4]	K07
DDR0B_DQ2[5]	J04
DDR0B_DQ2[6]	M05
DDR0B_DQ2[7]	H07
DDR0B_DQ3[0]	L02
DDR0B_DQ3[1]	K03
DDR0B_DQ3[2]	L04
DDR0B_DQ3[3]	M01
DDR0B_DQ3[4]	J02
DDR0B_DQ3[5]	K01
DDR0B_DQ3[6]	M03
DDR0B_DQ3[7]	H01
DDR0B_DQS0_c	P12
DDR0B_DQS0_t	N12
DDR0B_DQS1_c	P10
DDR0B_DQS1_t	N10
DDR0B_DQS2_c	P06
DDR0B_DQS2_t	N06
DDR0B_DQS3_c	P04
DDR0B_DQS3_t	N04
DDR0B_DQS4_c	P14
DDR0B_DQS4_t	N14

SIGNAL NAME	PIN NUMBER
DDR1B_DQ0[7]	D12
DDR1B_DQ1[0]	E09
DDR1B_DQ1[1]	C09
DDR1B_DQ1[2]	B10
DDR1B_DQ1[3]	D10
DDR1B_DQ1[4]	D08
DDR1B_DQ1[5]	B08
DDR1B_DQ1[6]	E11
DDR1B_DQ1[7]	C11
DDR1B_DQ2[0]	D06
DDR1B_DQ2[1]	B06
DDR1B_DQ2[2]	C05
DDR1B_DQ2[3]	E07
DDR1B_DQ2[4]	C07
DDR1B_DQ2[5]	B04
DDR1B_DQ2[6]	E05
DDR1B_DQ2[7]	A07
DDR1B_DQ3[0]	D02
DDR1B_DQ3[1]	C03
DDR1B_DQ3[2]	D04
DDR1B_DQ3[3]	E01
DDR1B_DQ3[4]	B02
DDR1B_DQ3[5]	C01
DDR1B_DQ3[6]	E03
DDR1B_DQ3[7]	A01
DDR1B_DQS0_c	G12
DDR1B_DQS0_t	F12
DDR1B_DQS1_c	G10
DDR1B_DQS1_t	F10
DDR1B_DQS2_c	G06
DDR1B_DQS2_t	F06
DDR1B_DQS3_c	G04
DDR1B_DQS3_t	F04
DDR1B_DQS4_c	G14
DDR1B_DQS4_t	F14
HSA_0	N02
HSA_1	F02
HSCL_0	P45
HSCL_1	G45
HSDA_0	N45
HSDA_1	F45
PWR_EN_0	P01

Table 6 — DDR5 Dual-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

SIGNAL NAME	PIN NUMBER
PWR_EN_1	G01
PWR_GOOD_0	N01
PWR_GOOD_1	F01
RESET0_n	P46
RESET1_n	G46
UNLOCK_0	P02
UNLOCK_1	G02

SIGNAL NAME	PIN NUMBER
RFU	F08, F39, G08, G39, N08, N39, P08, P39
VIN_BULK	E23, E24, F23, F24, G23, G24, M23, M24, N23, N24, P23, P24
VSSa	B01, B46, D01, D23, D24, D46, F21, F26, G21, G26, J01, J46, L01, L23, L24, L46, N21, N26, P21, P26
VSSb	A02, A06, A10, A14, A18, A22, A25, A29, A33, A37, A41, A45, B05, B09, B13, B17, B21, B24, B28, B32, B36, B40, B44, C02, C06, C10, C14, C18, C22, C25, C29, C33, C37, C41, C45, D05, D09, D13, D17, D21, D28, D32, D36, D40, D44, E02, E06, E10, E14, E18, E22, E25, E29, E33, E37, E41, E45, H02, H06, H10, H14, H18, H22, H25, H29, H33, H37, H41, H45, J05, J09, J13, J17, J21, J24, J28, J32, J36, J40, J44, K02, K06, K10, K14, K18, K22, K25, K29, K33, K37, K41, K45, L05, L09, L13, L17, L21, L28, L32, L36, L40, L44, M02, M06, M10, M14, M18, M22, M25, M29, M33, M37, M41, M45
VSSc	A04, A08, A12, A16, A20, A27, A31, A35, A39, A43, B03, B07, B11, B15, B19, B23, B26, B30, B34, B38, B42, C04, C08, C12, C16, C20, C27, C31, C35, C39, C43, D03, D07, D11, D15, D19, D26, D30, D34, D38, D42, E04, E08, E12, E16, E20, E27, E31, E35, E39, E43, F03, F05, F07, F09, F11, F13, F15, F17, F19, F28, F30, F32, F34, F36, F38, F40, F42, F44, G03, G05, G07, G09, G11, G13, G15, G17, G19, G28, G30, G32, G34, G36, G38, G40, G42, G44, H04, H08, H12, H16, H20, H27, H31, H35, H39, H43, J03, J07, J11, J15, J19, J23, J26, J30, J34, J38, J42, K04, K08, K12, K16, K20, K27, K31, K35, K39, K43, L03, L07, L11, L15, L19, L26, L30, L34, L38, L42, M04, M08, M12, M16, M20, M27, M31, M35, M39, M43, N03, N05, N07, N09, N11, N13, N15, N17, N19, N28, N30, N32, N34, N36, N38, N40, N42, N44, P03, P05, P07, P09, P11, P13, P15, P17, P19, P28, P30, P32, P34, P36, P38, P40, P42, P44

NOTES:

1. VSSa are ground pins that are populated in the Variations AXXX and BXXX of the CAMM2 connector.
2. VSSb and VSSc are ground pins that are populated in the Variation CXXX of the CAMM2 Connector. They are intended to improve crosstalk performance of the CAMM2 connector. JEDEC JC-11 defines the ground pin population requirements based on connector performance requirements.

3.7 LP5 Signal Descriptions

Table 7 — LP5 Signal Descriptions

Signal	Type	I/O Level	Function
CK_t CK_c	Input	VDDQ	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]	Input	VDDQ	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS[3:0]	Input	VDDQ	Chip Select: CS is part of the command code, and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.
DVFSQ_n	Input	1.8v	Optional support for Dynamic Voltage and Frequency Scaling of VDDQ as defined in JESD209-5B. Analog signal sets VDDQ voltage for power savings, controlled by SOC, and routed to PMIC input pin. Support strongly recommended when PMIC support is available. Pull up resistor to 1.8v is required on motherboard. 10K ohm resistor value is recommended.
DQ0[7:0] DQ1[7:0]	Input/ Output	VDDQ	Data Input/Output: Bi-directional data bus.
DQS[1:0]_t DQS[1:0]_c	Input/ Output	VDDQ	Data Strobe: Differential output clock signals from DRAM used to strobe data during a READ operation. DQS_t is also used as a DRAM input Parity pin for Writes with Link Protection enabled.
DMI[1:0]	Input	VDDQ	Data Mask Inversion: DMI achieves multiple functions such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and DMI is a bi-directional signal and each byte of data has a DMI signal.
GSI_n	Output	Open Drain	General Status Interrupt. When this pin is enabled, the PMIC asserts this pin low to communicate one or more events to host. This pin stays asserted until the appropriate PMIC registers are explicitly cleared and the event is no longer present. Pull up resistor to 1.8v is required on motherboard. 10K ohm resistor value is recommended.
GND_Detect _n	Output	GND or float	Optional support for Ground Detect. When low, rows R and T connect to a ground plane (occurs only in CAMM2 modules before v1.0 of this standard). When sampled high, rows R and T have floating pins unless otherwise defined in this standard. Pull up resistor on motherboard is required. Resistance and voltage level are system dependent.
VDDQ	Supply	0.27V- 0.57V	IO Buffer Power as defined in JESD209-5. Optional support for Common VDDQ delivery method defined in par. 4.3

Table 7 — LP5 Signal Descriptions (cont'd)

Signal	Type	I/O Level	Function
VDDQ_DISABLE	Input	VIN_BULK	Disable signal for PMIC VDDQ output. Optional support for Common VDDQ delivery method defined in par. 4.3
WCK[1:0]_t WCK[1:0]_c	Input	VDDQ	Data Clocks: Differential clocks used for WRITE data capture and READ data output.

NOTES:

1. Subchannel groups are represented with signal prefixes LPDDR0A_, LPDDR0B_, LPDDR0C_, LPDDR0D_, LPDDR1A_, LPDDR1B_, LPDDR1C, and LPDDR1D_. All of the above signals are duplicated for each subchannel.
2. DMI for LPDDR is high true while DMI_n for DDR is low true.

3.8 LP5 CAMM2 Connector Pin Assignments

3.9 LP5 Pinout Table

Table 8 — LP5 CAMM2 xxx Pin Connector Pin Wiring Assignment

SIGNAL NAME	PIN NUMBER
DVFSQ_n	A19
GND_Detect_n	R3
GSI_n	P35
HSA	P46
HSCL	H46
HSDA	A46
LPDDR0A_CA[0]	L12
LPDDR0A_CA[1]	K11
LPDDR0A_CA[2]	J10
LPDDR0A_CA[3]	H09
LPDDR0A_CA[4]	L10
LPDDR0A_CA[5]	K09
LPDDR0A_CA[6]	M09
LPDDR0A_CK_c	P10
LPDDR0A_CK_t	N10
LPDDR0A_CS[0]	H11
LPDDR0A_CS[1]	M11
LPDDR0A_CS[2]	H05
LPDDR0A_CS[3]	N12
LPDDR0A_DMI0	M07
LPDDR0A_DMI1	M03
LPDDR0A_DQ0[0]	J08
LPDDR0A_DQ0[1]	L08
LPDDR0A_DQ0[2]	H07
LPDDR0A_DQ0[3]	K07
LPDDR0A_DQ0[4]	L06
LPDDR0A_DQ0[5]	M05
LPDDR0A_DQ0[6]	K05
LPDDR0A_DQ0[7]	J06
LPDDR0A_DQ1[0]	K01
LPDDR0A_DQ1[1]	M01
LPDDR0A_DQ1[2]	J02
LPDDR0A_DQ1[3]	L02
LPDDR0A_DQ1[4]	K03
LPDDR0A_DQ1[5]	L04
LPDDR0A_DQ1[6]	J04
LPDDR0A_DQ1[7]	H03
LPDDR0A_DQS0_c	P08
LPDDR0A_DQS0_t	N08
LPDDR0A_DQS1_c	P02

SIGNAL NAME	PIN NUMBER
LPDDR1A_CA[0]	L35
LPDDR1A_CA[1]	K34
LPDDR1A_CA[2]	J33
LPDDR1A_CA[3]	H32
LPDDR1A_CA[4]	L33
LPDDR1A_CA[5]	K32
LPDDR1A_CA[6]	M32
LPDDR1A_CK_c	P33
LPDDR1A_CK_t	N33
LPDDR1A_CS[0]	H34
LPDDR1A_CS[1]	M34
LPDDR1A_CS[2]	H28
LPDDR1A_CS[3]	H24
LPDDR1A_DMI0	M30
LPDDR1A_DMI1	M26
LPDDR1A_DQ0[0]	J31
LPDDR1A_DQ0[1]	L31
LPDDR1A_DQ0[2]	H30
LPDDR1A_DQ0[3]	K30
LPDDR1A_DQ0[4]	M28
LPDDR1A_DQ0[5]	L29
LPDDR1A_DQ0[6]	K28
LPDDR1A_DQ0[7]	J29
LPDDR1A_DQ1[0]	M24
LPDDR1A_DQ1[1]	L25
LPDDR1A_DQ1[2]	K24
LPDDR1A_DQ1[3]	J25
LPDDR1A_DQ1[4]	K26
LPDDR1A_DQ1[5]	L27
LPDDR1A_DQ1[6]	J27
LPDDR1A_DQ1[7]	H26
LPDDR1A_DQS0_c	P31
LPDDR1A_DQS0_t	N31
LPDDR1A_DQS1_c	P25
LPDDR1A_DQS1_t	N25
LPDDR1A_WCK0_c	P29
LPDDR1A_WCK0_t	N29
LPDDR1A_WCK1_c	P27
LPDDR1A_WCK1_t	N27

Table 8 — LPDDR5/5X CAMM2 xxx Pin Connector Pin Wiring Assignment (cont'd)

SIGNAL NAME	PIN NUMBER
LPDDR0A_DQS1_t	N02
LPDDR0A_WCK0_c	P06
LPDDR0A_WCK0_t	N06
LPDDR0A_WCK1_c	P04
LPDDR0A_WCK1_t	N04
LPDDR0B_CA[0]	C09
LPDDR0B_CA[1]	E09
LPDDR0B_CA[2]	D10
LPDDR0B_CA[3]	A11
LPDDR0B_CA[4]	E11
LPDDR0B_CA[5]	C11
LPDDR0B_CA[6]	D12
LPDDR0B_CK_c	G10
LPDDR0B_CK_t	F10
LPDDR0B_CS[0]	A09
LPDDR0B_CS[1]	B10
LPDDR0B_CS[2]	F12
LPDDR0B_CS[3]	A05
LPDDR0B_DMI0	A03
LPDDR0B_DMI1	A07
LPDDR0B_DQ0[0]	C01
LPDDR0B_DQ0[1]	B02
LPDDR0B_DQ0[2]	E01
LPDDR0B_DQ0[3]	D02
LPDDR0B_DQ0[4]	C03
LPDDR0B_DQ0[5]	B04
LPDDR0B_DQ0[6]	D04
LPDDR0B_DQ0[7]	E03
LPDDR0B_DQ1[0]	D08
LPDDR0B_DQ1[1]	B08
LPDDR0B_DQ1[2]	E07
LPDDR0B_DQ1[3]	C07
LPDDR0B_DQ1[4]	B06
LPDDR0B_DQ1[5]	C05
LPDDR0B_DQ1[6]	D06
LPDDR0B_DQ1[7]	E05
LPDDR0B_DQS0_c	G02
LPDDR0B_DQS0_t	F02
LPDDR0B_DQS1_c	G08
LPDDR0B_DQS1_t	F08
LPDDR0B_WCK0_c	G04
LPDDR0B_WCK0_t	F04

SIGNAL NAME	PIN NUMBER
LPDDR1B_CA[0]	C32
LPDDR1B_CA[1]	E32
LPDDR1B_CA[2]	D33
LPDDR1B_CA[3]	A34
LPDDR1B_CA[4]	E34
LPDDR1B_CA[5]	C34
LPDDR1B_CA[6]	B35
LPDDR1B_CK_c	G33
LPDDR1B_CK_t	F33
LPDDR1B_CS[0]	A32
LPDDR1B_CS[1]	B33
LPDDR1B_CS[2]	G35
LPDDR1B_CS[3]	A24
LPDDR1B_DMI0	A26
LPDDR1B_DMI1	A30
LPDDR1B_DQ0[0]	C24
LPDDR1B_DQ0[1]	B25
LPDDR1B_DQ0[2]	E24
LPDDR1B_DQ0[3]	D25
LPDDR1B_DQ0[4]	B27
LPDDR1B_DQ0[5]	C26
LPDDR1B_DQ0[6]	D27
LPDDR1B_DQ0[7]	E26
LPDDR1B_DQ1[0]	C30
LPDDR1B_DQ1[1]	B31
LPDDR1B_DQ1[2]	E30
LPDDR1B_DQ1[3]	D31
LPDDR1B_DQ1[4]	B29
LPDDR1B_DQ1[5]	C28
LPDDR1B_DQ1[6]	D29
LPDDR1B_DQ1[7]	E28
LPDDR1B_DQS0_c	G25
LPDDR1B_DQS0_t	F25
LPDDR1B_DQS1_c	G31
LPDDR1B_DQS1_t	F31
LPDDR1B_WCK0_c	G27
LPDDR1B_WCK0_t	F27
LPDDR1B_WCK1_c	G29
LPDDR1B_WCK1_t	F29
LPDDR1C_CA[0]	M38
LPDDR1C_CA[1]	K38
LPDDR1C_CA[2]	L37

Table 8 — LPDDR5/5X CAMM2 xxx Pin Connector Pin Wiring Assignment (cont'd)

SIGNAL NAME	PIN NUMBER
LPDDR0B_WCK1_c	G06
LPDDR0B_WCK1_t	F06
LPDDR0C_CA[0]	M15
LPDDR0C_CA[1]	K15
LPDDR0C_CA[2]	L14
LPDDR0C_CA[3]	H13
LPDDR0C_CA[4]	K13
LPDDR0C_CA[5]	M13
LPDDR0C_CA[6]	J12
LPDDR0C_CK_c	P14
LPDDR0C_CK_t	N14
LPDDR0C_CS[0]	J14
LPDDR0C_CS[1]	H15
LPDDR0C_CS[2]	H19
LPDDR0C_CS[3]	H23
LPDDR0C_DMI0	M21
LPDDR0C_DMI1	M17
LPDDR0C_DQ0[0]	K23
LPDDR0C_DQ0[1]	M23
LPDDR0C_DQ0[2]	J22
LPDDR0C_DQ0[3]	L22
LPDDR0C_DQ0[4]	K21
LPDDR0C_DQ0[5]	L20
LPDDR0C_DQ0[6]	J20
LPDDR0C_DQ0[7]	H21
LPDDR0C_DQ1[0]	J16
LPDDR0C_DQ1[1]	L16
LPDDR0C_DQ1[2]	H17
LPDDR0C_DQ1[3]	K17
LPDDR0C_DQ1[4]	M19
LPDDR0C_DQ1[5]	L18
LPDDR0C_DQ1[6]	K19
LPDDR0C_DQ1[7]	J18
LPDDR0C_DQS0_c	P22
LPDDR0C_DQS0_t	N22
LPDDR0C_DQS1_c	P16
LPDDR0C_DQS1_t	N16
LPDDR0C_WCK0_c	P20
LPDDR0C_WCK0_t	N20
LPDDR0C_WCK1_c	P18
LPDDR0C_WCK1_t	N18
LPDDR0D_CA[0]	B12

SIGNAL NAME	PIN NUMBER
LPDDR1C_CA[3]	H36
LPDDR1C_CA[4]	K36
LPDDR1C_CA[5]	M36
LPDDR1C_CA[6]	J35
LPDDR1C_CK_c	P37
LPDDR1C_CK_t	N37
LPDDR1C_CS[0]	J37
LPDDR1C_CS[1]	H38
LPDDR1C_CS[2]	N35
LPDDR1C_CS[3]	H42
LPDDR1C_DMI0	M44
LPDDR1C_DMI1	M40
LPDDR1C_DQ0[0]	K46
LPDDR1C_DQ0[1]	M46
LPDDR1C_DQ0[2]	J45
LPDDR1C_DQ0[3]	L45
LPDDR1C_DQ0[4]	K44
LPDDR1C_DQ0[5]	L43
LPDDR1C_DQ0[6]	J43
LPDDR1C_DQ0[7]	H44
LPDDR1C_DQ1[0]	J39
LPDDR1C_DQ1[1]	L39
LPDDR1C_DQ1[2]	H40
LPDDR1C_DQ1[3]	K40
LPDDR1C_DQ1[4]	M42
LPDDR1C_DQ1[5]	L41
LPDDR1C_DQ1[6]	K42
LPDDR1C_DQ1[7]	J41
LPDDR1C_DQS0_c	P45
LPDDR1C_DQS0_t	N45
LPDDR1C_DQS1_c	P39
LPDDR1C_DQS1_t	N39
LPDDR1C_WCK0_c	P43
LPDDR1C_WCK0_t	N43
LPDDR1C_WCK1_c	P41
LPDDR1C_WCK1_t	N41
LPDDR1D_CA[0]	D35
LPDDR1D_CA[1]	C36
LPDDR1D_CA[2]	D37
LPDDR1D_CA[3]	C38
LPDDR1D_CA[4]	B37
LPDDR1D_CA[5]	E38

Table 8 — LPDDR5/5X CAMM2 xxx Pin Connector Pin Wiring Assignment (cont'd)

SIGNAL NAME	PIN NUMBER
LPDDR0D_CA[1]	C13
LPDDR0D_CA[2]	D14
LPDDR0D_CA[3]	C15
LPDDR0D_CA[4]	B14
LPDDR0D_CA[5]	E15
LPDDR0D_CA[6]	A15
LPDDR0D_CK_c	G14
LPDDR0D_CK_t	F14
LPDDR0D_CS[0]	E13
LPDDR0D_CS[1]	A13
LPDDR0D_CS[2]	A23
LPDDR0D_CS[3]	G12
LPDDR0D_DMI0	A17
LPDDR0D_DMI1	A21
LPDDR0D_DQ0[0]	D16
LPDDR0D_DQ0[1]	B16
LPDDR0D_DQ0[2]	E17
LPDDR0D_DQ0[3]	C17
LPDDR0D_DQ0[4]	B18
LPDDR0D_DQ0[5]	C19
LPDDR0D_DQ0[6]	D18
LPDDR0D_DQ0[7]	E19
LPDDR0D_DQ1[0]	C23
LPDDR0D_DQ1[1]	B22
LPDDR0D_DQ1[2]	E23
LPDDR0D_DQ1[3]	D22
LPDDR0D_DQ1[4]	B20
LPDDR0D_DQ1[5]	C21
LPDDR0D_DQ1[6]	D20
LPDDR0D_DQ1[7]	E21
LPDDR0D_DQS0_c	G16
LPDDR0D_DQS0_t	F16
LPDDR0D_DQS1_c	G22
LPDDR0D_DQS1_t	F22
LPDDR0D_WCK0_c	G18
LPDDR0D_WCK0_t	F18
LPDDR0D_WCK1_c	G20
LPDDR0D_WCK1_t	F20

SIGNAL NAME	PIN NUMBER
LPDDR1D_CA[6]	A38
LPDDR1D_CK_c	G37
LPDDR1D_CK_t	F37
LPDDR1D_CS[0]	E36
LPDDR1D_CS[1]	A36
LPDDR1D_CS[2]	A42
LPDDR1D_CS[3]	F35
LPDDR1D_DMI0	A40
LPDDR1D_DMI1	A44
LPDDR1D_DQ0[0]	D39
LPDDR1D_DQ0[1]	B39
LPDDR1D_DQ0[2]	E40
LPDDR1D_DQ0[3]	C40
LPDDR1D_DQ0[4]	B41
LPDDR1D_DQ0[5]	C42
LPDDR1D_DQ0[6]	D41
LPDDR1D_DQ0[7]	E42
LPDDR1D_DQ1[0]	C46
LPDDR1D_DQ1[1]	B45
LPDDR1D_DQ1[2]	E46
LPDDR1D_DQ1[3]	D45
LPDDR1D_DQ1[4]	B43
LPDDR1D_DQ1[5]	C44
LPDDR1D_DQ1[6]	D43
LPDDR1D_DQ1[7]	E44
LPDDR1D_DQS0_c	G39
LPDDR1D_DQS0_t	F39
LPDDR1D_DQS1_c	G45
LPDDR1D_DQS1_t	F45
LPDDR1D_WCK0_c	G41
LPDDR1D_WCK0_t	F41
LPDDR1D_WCK1_c	G43
LPDDR1D_WCK1_t	F43
PWR_EN	P01
PWR_GOOD	H01
RESET_n	A01
UNLOCK	A28
VDDQ_DISABLE	R24

Table 8 — LPDDR5/5X CAMM2 xxx Pin Connector Pin Wiring Assignment (cont'd)

SIGNAL NAME	PIN NUMBER
RFU	P12 plus optional pins R23, R44, T2, T45
VDDQ	All are optional pins: R1, R11, R13, R21, R26, R34, R36, R46, T1, T10, T12, T22, T25, T35, T37, T46
VIN_BULK	F23, F24, G23, G24, N23, N24, P23, P24
VSSa	B01, B46, D01, D23, D24, D46, F01, F21, F26, F46, G01, G21, G26, G46, J01, J46, L01, L23, L24, L46, N01, N21, N26, N46, P21, P26
VSSb	A02, A06, A10, A14, A18, A22, A25, A29, A33, A37, A41, A45, B05, B09, B13, B17, B21, B24, B28, B32, B36, B40, B44, C02, C06, C10, C14, C18, C22, C25, C29, C33, C37, C41, C45, D05, D09, D13, D17, D21, D28, D32, D36, D40, D44, E02, E06, E10, E14, E18, E22, E25, E29, E33, E37, E41, E45, F28, G28, H02, H06, H10, H14, H18, H22, H25, H29, H33, H37, H41, H45, J05, J09, J13, J17, J21, J24, J28, J32, J36, J40, J44, K02, K06, K10, K14, K18, K22, K25, K29, K33, K37, K41, K45, L05, L09, L13, L17, L21, L28, L32, L36, L40, L44, M02, M06, M10, M14, M18, M22, M25, M29, M33, M37, M41, M45
VSSc	A04, A08, A12, A16, A20, A27, A31, A35, A39, A43, B03, B07, B11, B15, B19, B23, B26, B30, B34, B38, B42, C04, C08, C12, C16, C20, C27, C31, C35, C39, C43, D03, D07, D11, D15, D19, D26, D30, D34, D38, D42, E04, E08, E12, E16, E20, E27, E31, E35, E39, E43, F03, F05, F07, F09, F11, F13, F15, F17, F19, F30, F32, F34, F36, F38, F40, F42, F44, G03, G05, G07, G09, G11, G13, G15, G17, G19, G30, G32, G34, G36, G38, G40, G42, G44, H04, H08, H12, H16, H20, H27, H31, H35, H39, H43, J03, J07, J11, J15, J19, J23, J26, J30, J34, J38, J42, K04, K08, K12, K16, K20, K27, K31, K35, K39, K43, L03, L07, L11, L15, L19, L26, L30, L34, L38, L42, M04, M08, M12, M16, M20, M27, M31, M35, M39, M43, N03, N05, N07, N09, N11, N13, N15, N17, N19, N28, N30, N32, N34, N36, N38, N40, N42, N44, P03, P05, P07, P09, P11, P13, P15, P17, P19, P28, P30, P32, P34, P36, P38, P40, P42, P44

NOTES:

1. VSSa are ground pins that are populated in the Variations AXXX and BXXX of the CAMM2 connector.
2. VSSb and VSSc are ground pins that are populated in the Variation CXXX of the CAMM2 Connector. They are intended to improve crosstalk performance of the CAMM2 connector. JEDEC JC-11 defines the ground pin population requirements based on connector performance requirements.
3. Optional pins above are associated with a revised CAMM2 connector that populates some of the RFU locations in rows R and T for use with VDDQ Common Power Delivery.

4 Power Details

4.1 CAMM2 Voltage Requirements

For the details and updates, please refer to the latest version of:

- JESD301-2: PMIC5100 Power Management IC Standard for DDR5
- JESD301-3: PMIC5200 Power Management IC Standard for LPDDR5.
    - Note: First LPDDR5 CAMM2 version may use PMIC5100 plus external voltage regulator (LDO or switcher) to produce VDDQ.

The CAMM2 has a PMIC on the PCB. All required voltages are generated by the PMIC from the VIN_BULK supply. The following is the typical use of PMIC outputs:

Table 9 — DDR5 (PMIC5100) and LP5 (PMIC5200) Voltage Rails

	DDR5		LP5		LP5	
PMIC	**PMIC5100**		**PMIC5100 + VR**		**PMIC5200**	
PMIC Rail	Power Connection	Nominal V_{out} (V)	Power Connection	Nominal V_{out} (V)	Power Connection	Nominal V_{out} (V)
SWA(1)	VDD	1.1	VDD2*	1.05	VDD2H	1.05
SWB(1)	VDDQ	1.1	VR* > VDDQ	0.5	VDDQ	0.5
SWC	VPP	1.8	VPP	1.8	VDD1 (VPP)	1.8
SWD					VDD2L	0.9
LDO_1P8V		1.8		1.8		1.8
LDO_1P0V		1.0		1.0		1.0
NOTE 1 SWA/B are dual phased and supply external VR for VDDQ.						

The initial CAMM2 design for LP5 shall implement a discrete dc-dc voltage regulator for VDDQ rail until an integrated solution is available. The VDD2L rail is not supported in this case, nor does the VDDQ rail support 0.3 V.

4.2 Soft Stop Time Programing for the PMIC Registers

To reduce the power line spike, the Soft Stop Time register setting for all PMIC output switch rails on module must be set to 0b11.

Table 10 — DDR5 PMIC5100 Register Setting for the Soft Stop

PMIC Register	Description	Register Bit	Value (binary)	Soft Stop Time (ms)
0x46	R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME	[1:0]	11	4
0x4A	R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME	[1:0]	11	4
0x4C	R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME	[1:0]	11	8

4.2 Soft Stop Time Programing for the PMIC Registers (cont'd)

Table 11 — LP5 PMIC5200 Register Setting for the Soft Stop

PMIC Register	Description	Register Bit	Value (binary)	Soft Stop Time(ms)
0x44 and 0x46	R44 [7]: SWA_OUTPUT_SOFT_STOP_TIME_EXTENSION and R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME	R44 [7] and R46 [1:0]	011	4
0x44 and 0x4A	R44 [5]: SWB_OUTPUT_SOFT_STOP_TIME_EXTENSION and R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME	R44 [5] and R4A [1:0]	011	4
0x44 and 0x4C	R44 [4]: SWC_OUTPUT_SOFT_STOP_TIME_EXTENSION and R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME	R44 [4] and R4C [1:0]	011	8
0x44 and 0x48	R44 [6]: SWD_OUTPUT_SOFT_STOP_TIME_EXTENSION and R48 [1:0]: SWD_OUTPUT_SOFT_STOP_TIME	R44 [6] and R48 [1:0]	011	4

4.3 LP5 VDDQ Power Delivery Methods

Two methods are defined for power delivery: split-rail and common. Support of the split-rail method is required while support of the common method is optional.

4.3.1 VDDQ Split-Rail Method

The Split-Rail method delivers VDDQ through separate voltage regulators to the SOC and DRAM. There is no connection or synchronization between voltage regulators VDDQa and VDDQb shown below.

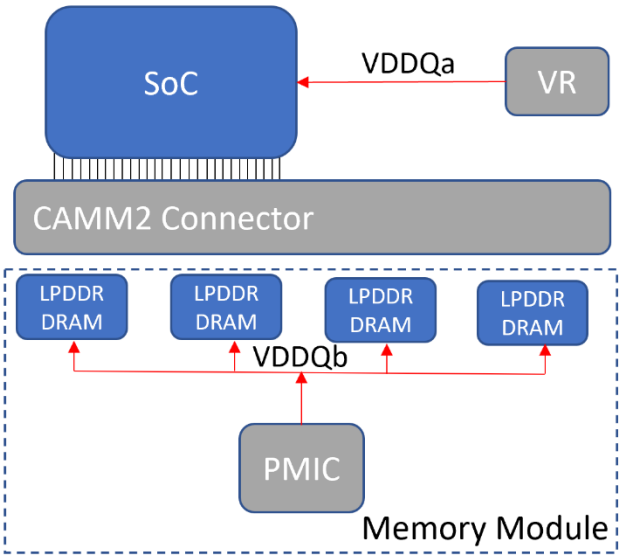


Figure 1 — LP5 CAMM2 VDDQ Split-Rail Power Delivery Method

4.3.1 VDDQ Split-Rail Method (cont'd)

The Split-Rail method has benefits of fewer connector pins and simple power delivery. Local power delivery is relieved from the power budgeting complication of DDR4 and prior generations. Validation is more straight-forward due to less dependency on system design.

The Split-Rail method has the drawback of voltage regulator drift within its output voltage tolerance, which is due to response time to changes in current demands and noise from the input source. One regulator can be at its maximum voltage limit while the other is at its minimum voltage limit. Since the IO drivers are highly influenced by their IO supply voltage, the IO signal voltage margin is affected. When bus speeds increase, the IO signal voltage margin naturally decreases. The margin impact from the regulators can erode critical margin, which then limits the possible memory bus speed.

4.3.2 VDDQ Common Method

The Common method delivers VDDQ through a single voltage regulator to provide both VDDQa and VDDQb depicted below.

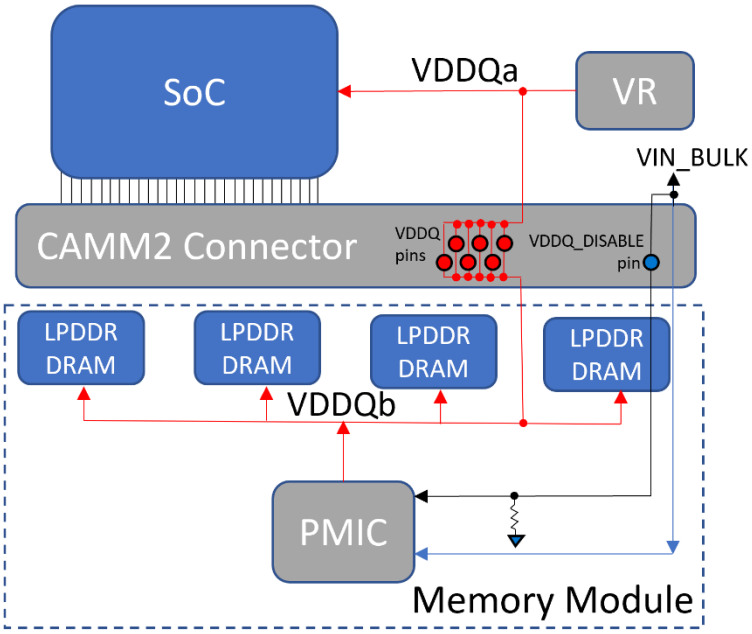


Figure 2 **— LP5 CAMM2 VDDQ Common Power Delivery Method**

VDDQ_DISABLE signal is tied directly to VIN_BULK to indicate to the PMIC whether it should enable or disable its VDDQ output.

- System boards designed with the Split-Rail method will not have VDDQ available on the CAMM2 connector pins and must float the VDDQ_DISABLE signal. This negates VDDQ_DISABLE through the pulldown resistor, which instructs the PMIC to supply local VDDQ.

4.3.2 VDDQ Common Method (cont'd)

- System boards designed with the Common method will supply VDDQ to the CAMM2 connector and must also tie VDDQ_DISABLE to VIN_BULK. This asserts VDDQ_DISABLE, which instructs the PMIC to not supply local VDDQ.

The Common method solves the Split-Rail drawback but creates a new drawback of voltage budget complexity. VDDQ voltage tolerance must now be allocated between the System board and memory module.

The CAMM2 voltage requirements and the SDRAM voltage requirements are not identical. There must be some allowance for a small voltage drop across the CAMM2. Table 12 defines the requirements for the Host at the CAMM footprint. Some modules have lower current requirements. Any specific module must meet the SDRAM voltage requirements for its worst-case supply currents.

Table 12 — LP5 VDDQ Operating Voltage

Range	Voltage Rating (V)			Maximum Expected Current (AMPS)	Notes
	Minimum	Typical	Maximum		
Spec Range 1	**0.477**	**0.507**	**0.577**	**TBD**	**1,2,4,6**
Spec Range 2	**0.272**	**0.302**	**0.372**	**TBD**	**1,3,4,5,6**

NOTE 1 DC to 2 MHz voltage range includes all noise at System Board CAMM footprint, both DC and AC ripple fluctuations. Minimum, Typical, Maximum values plus 7mV (Range 1) and 2 mV (Range 2) to allow for connector and module power plane voltage drops.

NOTE 2 SPEC Range 1 is intended for IO operation with both ODT enabled and disabled.

NOTE 3 SPEC Range 2 is intended for IO operation with ODT disabled.

NOTE 4 IO operation at VDDQ levels between outside SPEC Range 1 or SPEC Range 2 is allowed with ODT disabled.

NOTE 5 Allowable range is valid only when DVFSQ is enabled.

NOTE 6 60 mV tolerance (-30 mV/+30 mV) is applied to VDDQ allowable ranges. Refer to Figure 191 VDDQ tolerance definition in allowable range.

Pin Usage Rules

- When an LP5 CAMM2 supports ONLY the Split-Rail method, it must not connect to the LP5 CAMM2 VDDQ pins.
- When an LP5 CAMM2 supports BOTH the Split-Rail and Common method, it MUST:
  - Connect to the VDDQ pins to receive voltage delivery from the system board
  - Connect to the VDDQ_DISABLE pin so that the system has ability to enable/disable the VDDQ generation within the module
- There are no cases where the CAMM2 module drives VDDQ onto the system board

5 Component Details

5.1 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for SDRAM signals. Decoupling capacitors for SDRAM devices must be located near the device power pins.

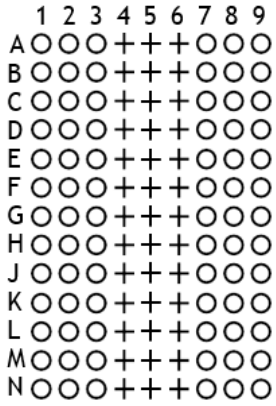
All DRAM components within an assembled CAMM2 must be sourced from the same manufacturer and must be the same silicon revision level.

Table 13 — DDR5 x8 SDRAM Pad Array

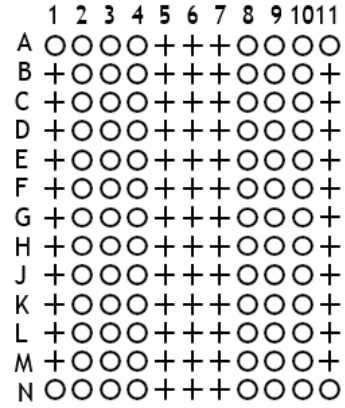
	1	2	3	4	5	6	7	8	9	10	11	
		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD		B
C		VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS		C
D		VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ		D
E		VDD	DQ4	DQ6				DQ7	DQ5	VDD		E
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS		F
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		G
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		H
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ		J
K		VDD	CA6	CA2				CA3	CA7	VDD		K
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ		L
M		CAI	CA10	CA12				CA13	CA11	RESET_n		M
N	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	N

DDR5 CAMM reference design uses the pad array with support balls.

MO-210-AL (x8)



MO-210-AN (x8) with support balls



O Populated ball
+ Ball not populated

NOTE 1 Additional columns and rows of inactive balls in MO-210 Terminal Pattern AN(x8) with support balls are for mechanical support only and should not be tied to either electrically high or low.
NOTE 2 Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.
NOTE 3 Please refer to the latest version of JESD79-5: DDR5 SDRAM specification for updates.

5.1 Component Types and Placement (cont'd)

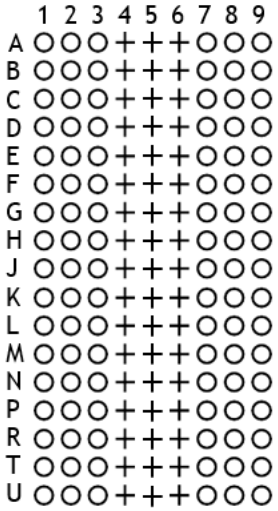
Table 14 — DDR5 x16 SDRAM Pad Array

1	2	3	4	5	6	7	8	9	10	11
	1	2	3	4	5	6	7	8	9	

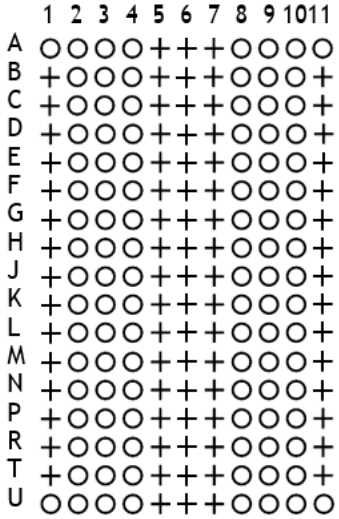
A	DNU	LBDQ	VSS	VPP	A
B		VDD	VDDQ	DQU2	B
C		VSS	DQU0	DQSU_P	C
D		VDDQ	VSS	DQSU_N	D
E		VDD	DQU4	DQU6	E
F		VDD	VDDQ	DQL2	F
G		VSS	DQL0	DQSL_P	G
H		VDDQ	VSS	DQSL_N	H
J		VDD	DQL4	DQL6	J
K		VSS	VDDQ	VSS	K
L		CA_ODT	MIR	VDD	L
M		ALERT_n	VSS	CS_n	M
N		VDDQ	CA4	CA0	N
P		VDD	CA6	CA2	P
R		VDDQ	VSS	CA8	R
T		CAI	CA10	CA12	T
U	DNU	VDD	VSS	VDD	U

A	ZQ	VSS	LBDQS	DNU
B	DQU3	VDDQ	VDD	
C	DMU_n	DQU1	VSS	
D	RFU	VSS	VDDQ	
E	DQU7	DQU5	VDD	
F	DQL3	VDDQ	VDD	
G	DML_n	DQL1	VSS	
H	RFU	VSS	VDDQ	
J	DQL7	DQL5	VDD	
K	VSS	VDDQ	VSS	
L	CK_t	VDDQ	TEN	
M	CK_c	VSS	VDD	
N	CA1	CA5	VDDQ	
P	CA3	CA7	VDD	
R	CA9	VSS	VDDQ	
T	CA13	CA11	RESET_n	
U	VPP	VSS	VDD	DNU

MO-210-AT (x16)



MO-210-AU (x16) with support balls



○ **Populated ball**
\+ **Ball not populated**

NOTE 1 Additional columns and rows of inactive balls in MO-210 Terminal Pattern AU(x16) with support balls are for mechanical support only and should not be tied to either electrically high or low.
NOTE 2 Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.
NOTE 3 Please refer to the latest version of JESD79-5: DDR5 SDRAM standard for updates.

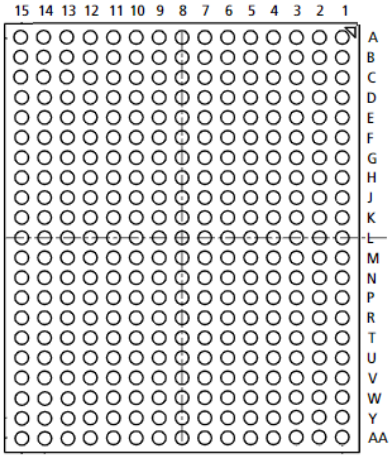
5.1 Component Types and Placement (cont'd)

Table 15 — LP5 x32 SDRAM Pad Array

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	VDDQ	DMI0_A	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI1_A	VDDQ	NC	NC	A
B	NC	VDDQ	RDQS0_t_A	VSS	DQ4_A	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ12_A	VSS	RDQS1_t_A	VDDQ	NC	B
C	VDD1	DQ1_A	VDDQ	RDQS0_c_A	VSS	DQ5_A	VDD2H	VSS	VDD2H	DQ13_A	VSS	RDQS1_c_A	VDDQ	DQ9_A	VDD1	C
D	DQ0_A	VSS	DQ3_A	VDDQ	WCK0_c_A	VSS	VSS	VDD2H	VSS	VSS	WCK1_c_A	VDDQ	DQ11_A	SS	DQ8_A	D
E	VSS	DQ2_A	VSS	WCK0_t_A	VDDQ	DQ6_A	VDD2H	VSS	VDD2H	DQ14_A	VDDQ	WCK1_t_A	VSS	DQ10_A	VSS	E
F	VDDQ	VSS	VDDQ	VDDQ	DQ7_A	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ15_A	VDDQ	VDDQ	VSS	VDDQ	F
G	VDDQ	VDDQ	VSS	CA0_A	VSS	CS1_A	VSS	CA2_A	VSS	CA4_A	VSS	CA6_AVSS	VSS	VDDQ	VDDQ	G
H	RESET_n	VDD2L	VSS	VSS	CA1_A	VSS	CS0_A	VSS	CK_t_A	VSS	CA3_A	VSS	CA5_A	VDD2L	ZQ_A	H
J	VSS	VDD2L	VSS	RFU CS3_A	VDD2H	RFU CS2_A	VSS	VSS	CK_c_A	VSS	VDD2H	VSS	VSS	VDD2L	VSS	J
K	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	K
L	VSS	VSS	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VSS	VSS	L
M	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	M
N	VSS	VDD2L	VSS	VSS	VDD2H	VSS	CK_c_B	VSS	VSS	VSS	VDD2H	VSS	VSS	VDD2L	VSS	N
P	RFU CS2_B	VDD2L	CA5_B	VSS	CA3_B	VSS	CK_t_B	VSS	CS0_B	VSS	CA1_B	VSS	VSS	VDD2L	RFU CS3_B	P
R	VDDQ	VDDQ	VSS	CA6_B	VSS	CA4_B	VSS	CA2_B	VSS	CS1_B	VSS	CA0_B	VSS	VDDQ	VDDQ	R
T	VDDQ	VSS	VDDQ	VDDQ	DQ15_B	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ7_B	VDDQ	VDDQ	VSS	VDDQ	T
U	VSS	DQ10_B	VSS	WCK1_t_B	VDDQ	DQ14_B	VDD2H	VSS	VDD2H	DQ6_B	VDDQ	WCK0_t_B	VSS	DQ2_B	VSS	U
V	DQ8_BVSS	VSS	DQ11_B	VDDQ	WCK1_c_B	VSS	VSS	VDD2H	VSS	VSS	WCK0_c_B	VDDQ	DQ3_B	VSS	DQ0_B	V
W	VDD1	DQ9_B	VDDQ	RDQS1_c_B	VSS	DQ13_B	VDD2H	VSS	VDD2H	DQ5_B	VSS	RDQS0_c_B	VDDQ	DQ1_B	VDD1	W
Y	NC	VDDQ	RDQS1_t_B	VSS	DQ12_B	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ4_B	VSS	RDQS0_t_B	VDDQ	NC	Y
AA	NC	NC	VDDQ	DMI1_B	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI0_B	VDDQ	NC	NC	AA

NOTE 1 RFU pins in red text are CS signals for 128GB support, where J4 = CS3_A, J6 = CS2_A, P1 = CS2_B, P15 = CS3_B

NOTE 2 JEDEC MO-338A for 315-ball terminal pattern



5.2 Decoupling Guidelines

Table 16 — DDR5 Decoupling Capacitor Guidelines

	Guideline	Note
VDD	Minimum of two decoupling capacitors to VSS per SDRAM, average of 30 µF per DRAM is recommended	Should be placed as close as possible to the DRAM VDD ball
VDDQ	Minimum of two decoupling capacitors to VSS per SDRAM, average of 7.5 µF per DRAM is recommended	Should be placed as close as possible to the DRAM VDDQ ball
VPP	Minimum of one decoupling cap per DRAM VPP pin, average of 3.5 µF per DRAM is recommended	Should be placed as close as possible to the DRAM VPP ball
VIN_BULK	Near the PMIC input : 6 pcs of 22 µF, 3 pcs of 0.1 µF Near CAMM2 connector VIN_BULK pins: 4 pcs of 22 µF, 2 pcs of 0.1 µF	

NOTES:

1. Decoupling capacitor values for VDD, VDDQ, and VPP vary by module and may be staggered to achieve best overall impedance vs. frequency response.
2. Recommended values for decoupling for VDD, VDDQ and VPP are 1 µF, 2.2 µF, 4.7 µF, and 1 µF.
3. Depending on the DRAM package size, all placements may not be possible.
4. Refer to PMIC specifications for details on decoupling around the PMIC chip.

Table 17 — LP5 Decoupling Capacitor Guidelines

	Guideline	Note
VDD1	Average of 5 µF per DRAM is recommended	Should be placed as close as possible to the DRAM VDD1 ball
VDD2H	Average of 15 µF per DRAM is recommended	Should be placed as close as possible to the DRAM VDD2H ball. If VDD2H and VDD2L are joined as one rail, add the two capacitances for that rail.
VDD2L	Average of 15 µF per DRAM is recommended	Should be placed as close as possible to the DRAM VDD2L ball
VDDQ	Average of 5 µF per DRAM is recommended	Should be placed as close as possible to the DRAM VDDQ ball
VIN_BULK	Near the PMIC input : 8 pcs of 22 µF, 4 pcs of 0.1 µF Near CAMM2 connector VIN_BULK pins: 6 pcs of 0.1µF	

NOTES:

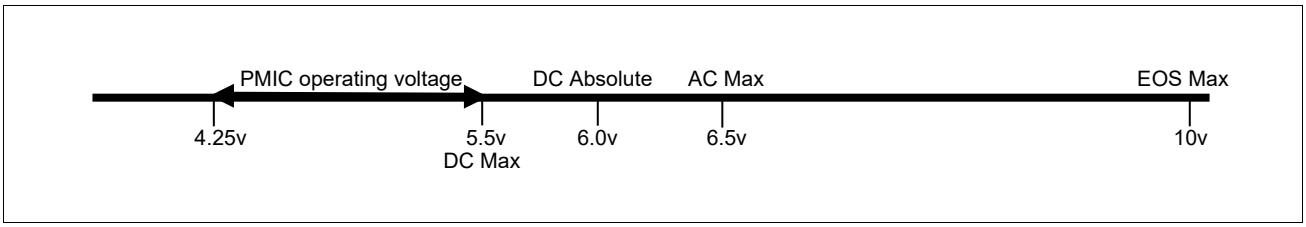
1. Decoupling capacitor values for VDD2H/L, VDDQ and VDD1 vary by module and may be staggered to achieve best overall impedance vs. frequency response.
2. Recommended values for decoupling for VDDH/L, VDDQ and VDD1 are 1 µF, 2.2 µF, 4.7 µF, and 10 µF.
3. Depending on the DRAM package size, all placements may not be possible.
4. Refer to PMIC specifications for details on decoupling around the PMIC chip.

5.3 Protection with TVS

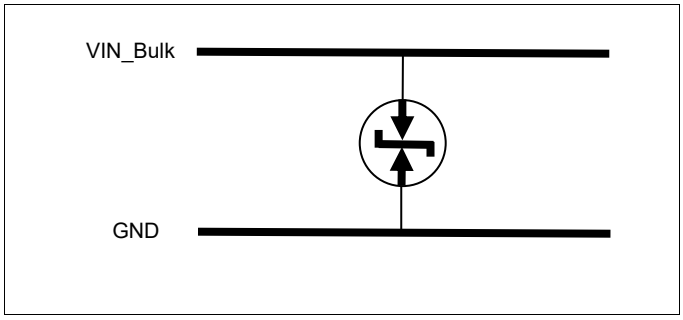
A Transient Voltage Suppression (TVS) diode must be included on the VIN_Bulk power rail for all CAMM2 designs with the following component specifications:

Power	PKG Size	Direction	VRWM (V, Min)	VRWM (V, Nom)
VIN_Bulk (5V)	0402	Unidirectional or Bi-directional	5.5	6

This component provides protection to the Client PMIC component which has these characteristics:



TVS Circuit Design:



6 CAMM2 Design Details

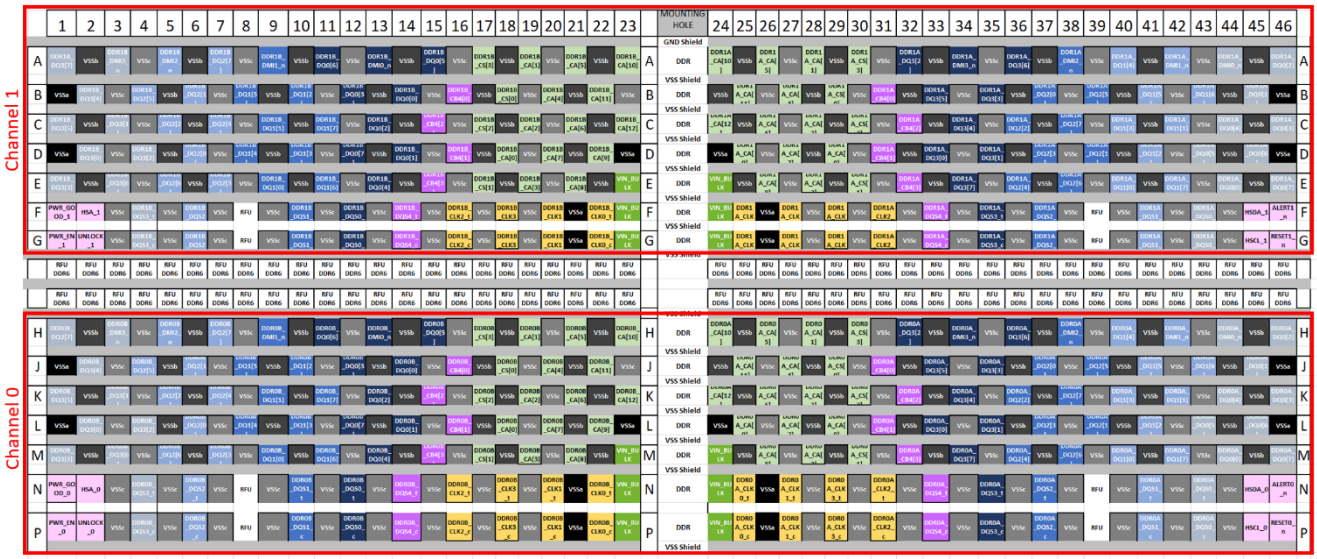
6.1 Channel Definition

This standard defines channels and subchannels as follows:

- A channel has a 64-bit data interface with varying number of subchannels.
  - With ECC support, the channel becomes 72-bits wide
  - A DDR5 channel consists of two 32-bit subchannels
  - An LP5 channel consists of four 16-bit subchannels
- A subchannel operates independent of any other subchannel, with its own clock, command, address, chip selects, and data signaling.

6.2 Single-channel versus Dual-channel DDR CAMM2

Single-channel BXXX CAMM2 connector contains half the pins of the AXXX CAMM2 connector. The connector is organized as Channel 0 in the lower portion of the pin array and Channel 1 in the upper portion of the pin array. Single-channel CAMM2 supports 64-bit data width, which is two 32-bit subchannels.



Dual-channel CAMM2 contains all the pins of the CAMM2 connector. Dual-channel CAMM2 supports 128-bit data width, which is four 32-bit subchannels.

The distinction between single-channel and dual-channel CAMM2s is important for mechanical stacking. Dual-channel CAMM2s cannot be stacked, while single-channel CAMM2s can be stacked as depicted in Figure 3.

6.2 Single-channel versus Dual-channel DDR CAMM2 (cont'd)

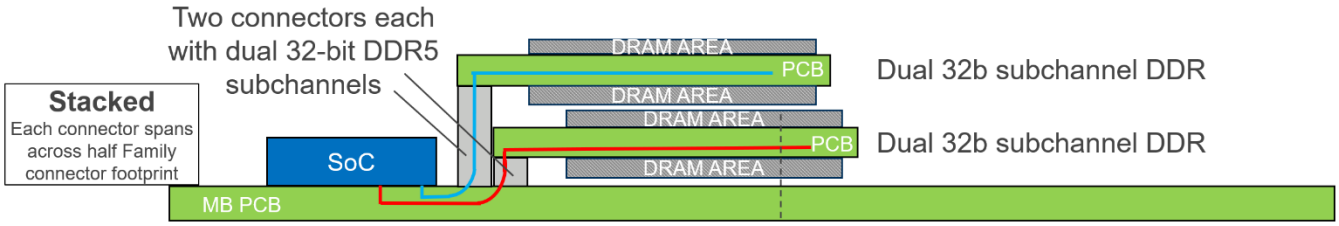


Figure 3 — Stacking with Single-channel CAMM2

Stacking allows system memory to be packaged within the system by increasing height of the volume needed for memory to save space in the Y direction. This is generally done for max capacity systems.

Dual-channel CAMM2s cover the entire CAMM2 connector, so they cannot be stacked. Figure 2 shows a side view of typical dual-channel CAMM2 mounting.

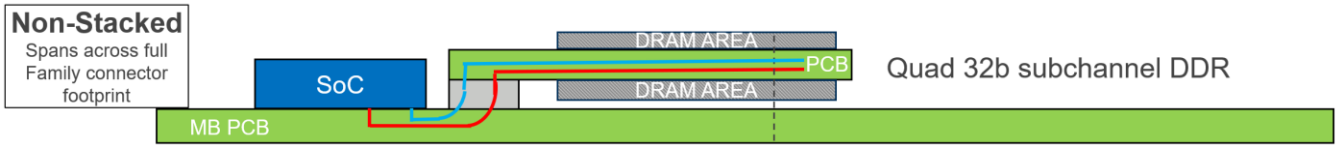


Figure 4 — Mounting of a Dual-channel CAMM2 with DDR5 DRAM

A dual-channel CAMM2 using LP5 DRAM covers the entire connector and places the LPDDR5/5X DRAM on top of the connector to minimize the motherboard area required for memory. A side view of an LPDDR5 CAMM2 is shown in Figure 3.

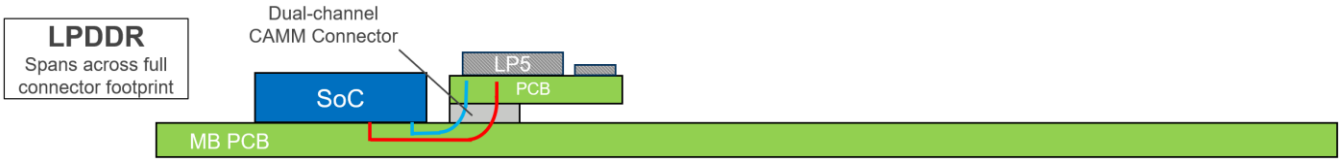


Figure 5 — Mounting of a Dual-channel CAMM2 with LP5 DRAM

6.3 Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for CAMM2 designs. The diagrams should be used to determine individual signal wiring on a memory module for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators "TL") represent physical trace segments. All other lines are zero in length. To verify CAMM2 functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. A typical data net structure is shown in Figure 6.

6.3 Explanation of Net Structure Diagrams (cont'd)

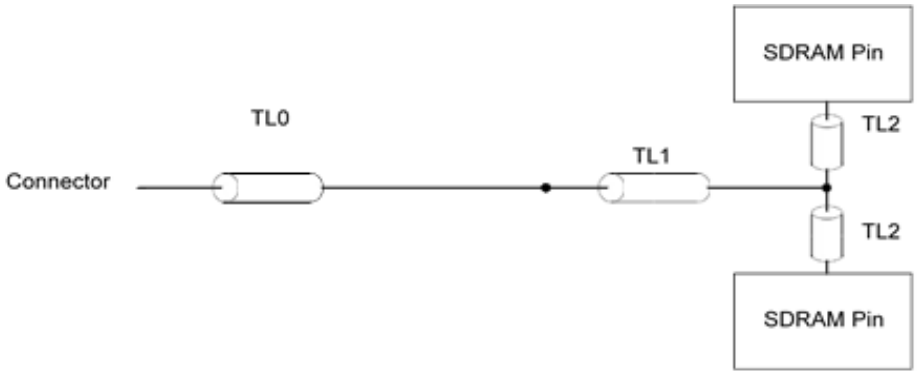


Figure 6 — Net Structure Example for Two Rank CAMM2

6.4 General Net Simulation Assumptions

To use simulation almost exclusively, some conditions must be defined so that the same conclusion is reached using different simulation tools.

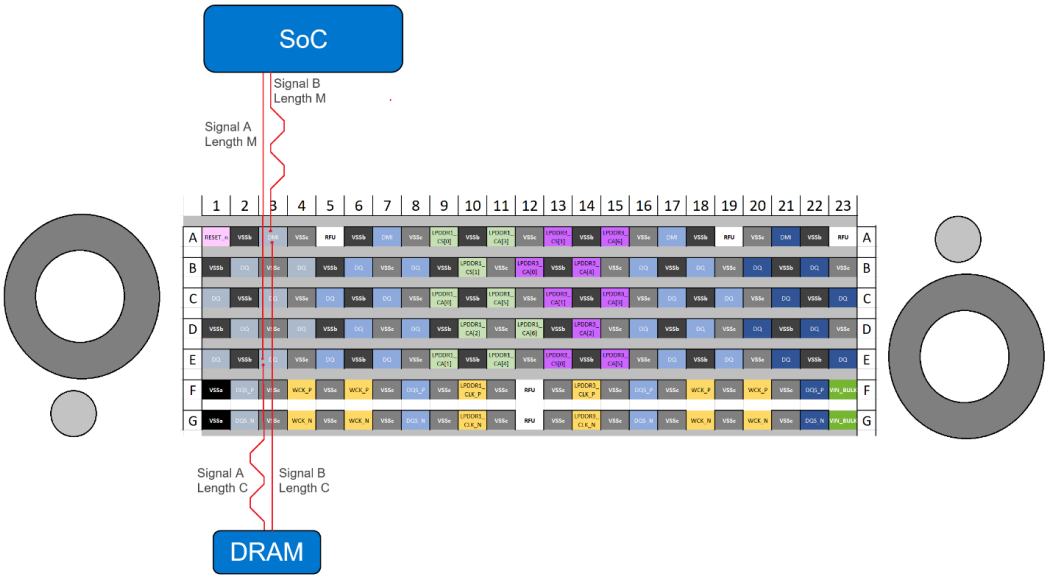
Table 18 — Simulation Conditions Example

Group	Parameter	Condition
Data Bus	Motherboard Length	40 mm
	Motherboard Impedance	40 Ω (75 Ω differential for Strobes)
	Motherboard Configuration	One CAMM2 supports all channels
	Routing Type	Stripline (Micro-strip)
	Driver	34 Ω DRAM with DRAM package
Command/Address, Chip Select	Motherboard Length	40 mm
	Motherboard Impedance	40 Ω (single ended)
	Motherboard Configuration	One CAMM2 supports all channels
	Driver	34 Ω DRAM with DRAM package
Clock	Motherboard Length	40 mm
	Motherboard Impedance	45 Ω differential for DDR 75 Ω differential for LPDDR
	Motherboard Configuration	One CAMM2 supports all channels
	Driver	75 Ω DRAM with DRAM package
NOTE Trace lengths above do not include pin offset adder as described in paragraph 6.5.		

6.5 CAMM2 Length-matching Principles

Traditional memory length-matching treats the motherboard and module routings separately. This works for UDIMM and SODIMM because the connector pins are lined in two rows. For CAMM2, the connector pin are lined in 14 rows, creating an array of pins. Length-matching within a data group can now span across multiple rows, which creates a new factor which must be considered. For example, traditional length-matching rules would force motherboard serpentining (aka meandering) on signal B to match signal A. Likewise, traditional rules would force module serpentining on signal A to match signal B. Since the data group spans across 5 rows and the rows are at 1mm pitch, then 4mm of trace length is unnecessarily added.to the data group.

6.5.1 Principle #1



Incorporate a trace length offset based on pin assignment within the connector array.

- Row A gets no offset
- Row B length offset = 1 mm
- Row C length offset = 2 mm
- Row D length offset = 3 mm
- Row E length offset = 4 mm
- Row F length offset = 5 mm
- Row H gets no offset
- Row J length offset = 1 mm
- Row K length offset = 2 mm
- Row L length offset = 3 mm
- Row M length offset = 4 mm
- Row N length offset = 5 mm

For example, if a data group has signals in rows A-F and the board designer selects signal C as the “target”, then all other signals are matched as follows:

- Signal A in row A = (length of C) – 2 mm
- Signal B in row B = (length of C) – 1 mm
- Signal C in row C = (length of C)
- Signal D in row D = (length of C) + 1 mm
- Signal E in row E = (length of C) + 2 mm
- Signal F in row F = (length of C) + 3 mm

6.5.2 Principle #2

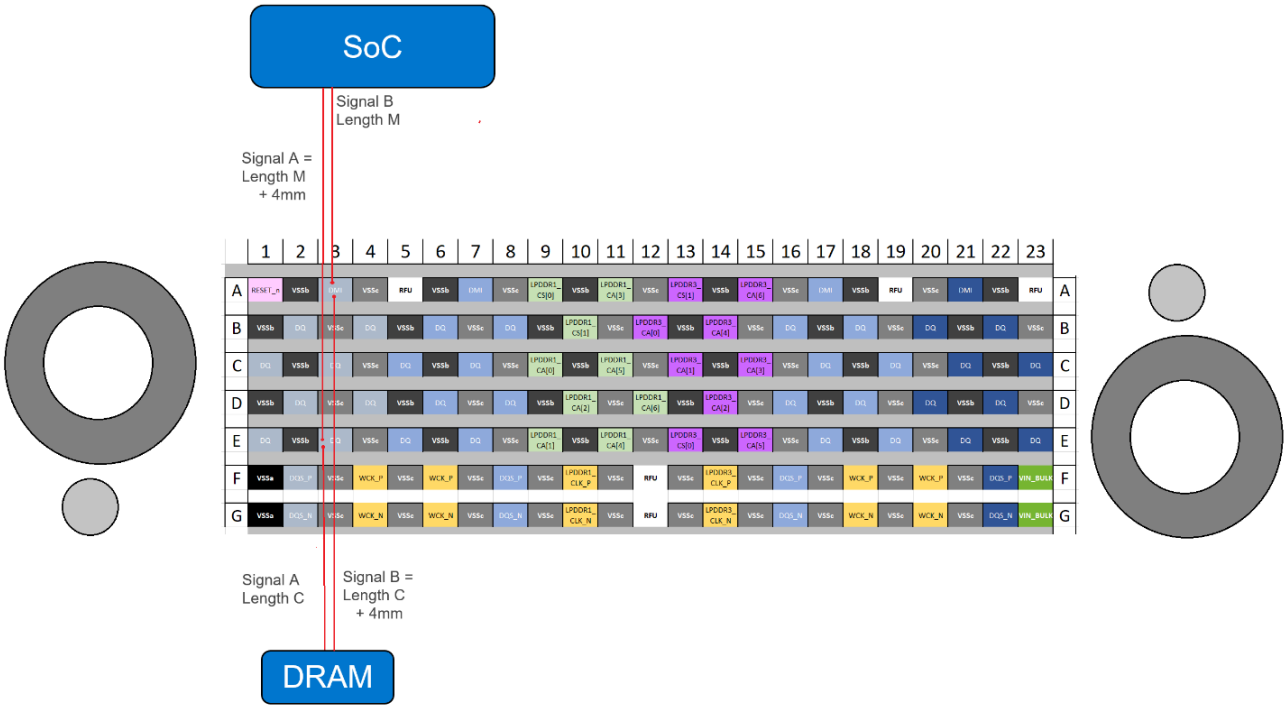
Data groups within a subchannel must be assigned within rows A-E or H-M (and cannot traverse across these row groupings.

6.5.3 Principle #3

Associated differential pairs (DQS, WCK, CK) must be assigned to

- rows F-G for data groups within rows A-E
- rows N-P for data groups within rows H-M

With these principles, the unnecessary serpentining can be removed, resulting in straighter traces.

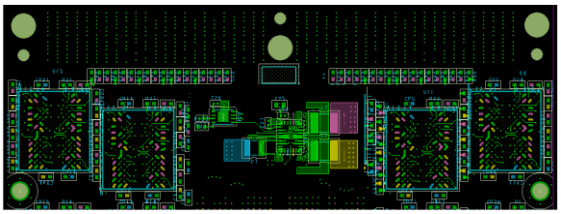


6.5.4 Principle #4

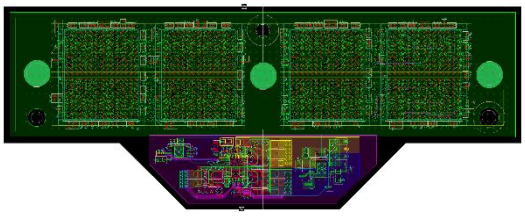
Trace length offsets are applied to DDR5 and LP5 designs.

- Even though the LP5 DRAM may have no offset when positioned above the CAMM2 connector, for the sake of minimal routing on the motherboards, these trace length offsets are applied to LP5 CAMM2.
- There is no negative consequence to applying trace length offsets to LP5. The alternative is forced length-matching within the motherboard (the traditional way) which would add unnecessary length. Even though the LP5 CAMM2 could be length matched without consequence within itself, the motherboard would still be compromised with extra length. This is avoided by applying trace length offsets to LP5 CAMM2.

6.5.4 Principle #4 (cont'd)



DDR5 CAMM2



LP5 CAMM2

6.5.5 Principle #5

Trace length ranges are set based on a variety of SoCs and do not reflect any particular SoC guideline. The goal is to establish a common set of CAMM2 length matching rules.

6.6 Length Matching Groups

The following length matching groups apply only to the CAMM2 designs (not system boards). The full channel length matching requirements depend on SOC requirements which shall be defined by each SOC supplier.

The length matching rules below must be used in concert with the pin offsets described above. Examples may make the process clearer.

1. Consider rule #5 in Table 19. Since all differential pairs of a subchannel are assigned to pins on rows F-G or N-P, there is no length offset due to pin assignments. Thus, CK differential pairs can be directly matched because there is no pin offset relative to signals within the match group.
2. Consider rule #2 in Table 19. The DQ bits within a byte lane are matched very tightly to their respective DQS. From an Allegro Constraint Manager viewpoint, the following approach is a good practice.

    a. A "target" signal is selected by the board designer. All other signals within the group shall be length-matched to the target. Commonly, the DQS_t signal is used as the target.

    b. The Calculated Offset is the distance from the target to the signal to be matched. If the target is at offset = 1 and the signal is at offset 6, the difference is 5. For example, this is why DMI0_n shows a Delta: Tolerance of 5 mm:0.025 mm. The delta of 5 mm comes from the row offset locations while the tolerance comes from rule #2.

6.6 Length Matching Groups (cont'd)

Table 19 — Allegro Constraint Manager Length Matching Example

CM Name	Applied Rule #	Calculated Offset	Delta Tolerance Min	Delta Tolerance Rule	Delta Tolerance Max	Delta: Tolerance Concatenation
J1.H44:U1.C8 [DDR0_DMI0_n]	2	6	-0.025	< (DQ-DQS) <	0.025	5 mm:0.025 mm
J1.P43:U1.D4 [DDR0_DQS0_c]	3	0	0	<	0.0625	0 mm:0.03125 mm
J1.N43:U1.C4 [DDR0_DQS0_t]	TARGET	1	-0.025	< (DQ-DQS) <	0.025	TARGET
J1.M44:U1.C3 [DDR0_DQ0[0]]	2	2	-0.025	< (DQ-DQS) <	0.025	1 mm:0.025 mm
J1.J45:U1.B4 [DDR0_DQ0[1]]	2	5	-0.025	< (DQ-DQS) <	0.025	4 mm:0.025 mm
J1.H46:U1.C9 [DDR0_DQ0[2]]	2	6	-0.025	< (DQ-DQS) <	0.025	5 mm:0.025 mm
J1.K46:U1.B8 [DDR0_DQ0[3]]	2	4	-0.025	< (DQ-DQS) <	0.025	3 mm:0.025 mm
J1.K44:U1.E4 [DDR0_DQ0[4]]	2	4	-0.025	< (DQ-DQS) <	0.025	3 mm:0.025 mm
J1.L43:U1.E3 [DDR0_DQ0[5]]	2	3	-0.025	< (DQ-DQS) <	0.025	2 mm:0.025 mm
J1.L45:U1.E8 [DDR0_DQ0[6]]	2	3	-0.025	< (DQ-DQS) <	0.025	2 mm:0.025 mm
J1.M46:U1.E9 [DDR0_DQ0[7]]	2	2	-0.025	< (DQ-DQS) <	0.025	1 mm:0.025 mm

Table 20 — Length-matching Groups for DDR5 CAMM2

#	Length Matching Groups	CAMM2 Bounds (mm)		
1	CA/CS matched to CK from connector to first DRAM	-16	< (CK_t- (CMD/CA/CS) <	10
2	DM, DQ and DQS within byte	-0.025	< (DQ-DQS_t) <	0.025
3	DQS and DQS#		<	0.0625
4	CK_t and CK_c		<	0.0625
5	CK0 and CK1 CK2 and CK3		<	0.3
6	CS and CK(1)	-0.0025	< (CK_t-CS) <	0.0025
7	All CS within each channel		<	0.125
8	CA and CK(1)	-1.2	< (CK_t-CMD) <	1.2
9	All CA within each channel		<	0.125
NOTE 1	Excluding initial length from connector to first DRAM. When DRAM is mirrored within same subchannel, rules 8 and 9 may be difficult to meet without excessive serpetining due to DRAM pinout. These designs may deviate with explanation in the raw card documentation.			

6.6 Length Matching Groups (cont'd)

Table 21 — Length-matching Specifications for LP5 CAMM2

#	Length Matching Groups	CAMM2 Bounds (mm)		
1	DQ and WCK per x16	-2	< (DQ - WCK_t) <	3.2
2	DQ and DQS per x8	-0.6	< (DQ - DQS_t) <	0.6
3	WCK and CK per x16	-1	< (WCK_t - CK_t) <	2
4	DQ signals per x8		<	0.025
5	Channel-to-channel CKs		<	5
6	CK and CA bits per x16	-1	< (CK_t-CA) <	1
7	CA bits per x16		<	0.025
8	CK and CS per x16*	-2.5	< (CK_t-CS) <	2.5
9	CS bits per x16		<	2
10	DQS_c and DQS_t		<	0.05
11	WCK_c and WCK_t		<	0.05
12	CK_c and CK_t		<	0.05

NOTES:

- * CS2 and CS3 are used only for heavily loaded LP5 CAMM2s which are expected to run at lower bus speed, therefore rule 8 can be relaxed to an additional +/- 2.5 mm for CS2 and CS3. This is needed due to pin assignment of CS2 and CS3 which cause those nets to be longer.
- Where groups are matched to a differential pair, the positive side of the differential pair is used as the Target
- The above CAMM2 Bounds are agreed by TG consensus as a starting point, but they are subject to change based on actual design in the coming months. The 1.0 version of this standard will lock these CAMM2 Bounds, however exceptions will continue to be allowed by TG concensus until CAMM2 designs mature.

6.7 Routing Considerations

6.7.1 CK, CMD/ADR, and CS Groups

The DDR5 modules implement a fly-by topology for routing CK, Command/Address and chip select signal groups. The Command/Address and Chip Select groups on DDR5 modules are length/delay matched to CK, between the connector and each SDRAM. Table provides a summary of the length/delay matching rules associated with the CK, Command/Address and chip select groups.

Clock drivers (CKD) are implemented to improve the subchannel timing/voltage margins. This causes a redefinition of the first clock length that is used for length matching. The first CK segment is defined as trace lengths of DCK_A + QCK_A, or DCK_B + QCK_B. The propagation delay through CKD is not included in length/delay matching calculations.

- DCK_A and DCK_B lengths extend from CAMM2 pin to CKD input pin
- QCK_A and QCK_B lengths extend from CKD output pin to first DRAM CK input pin.

For the length tables in the Annexes where there is not a specified tolerance, and the tolerance is not covered, a value of ± 1.0 mm shall be used.

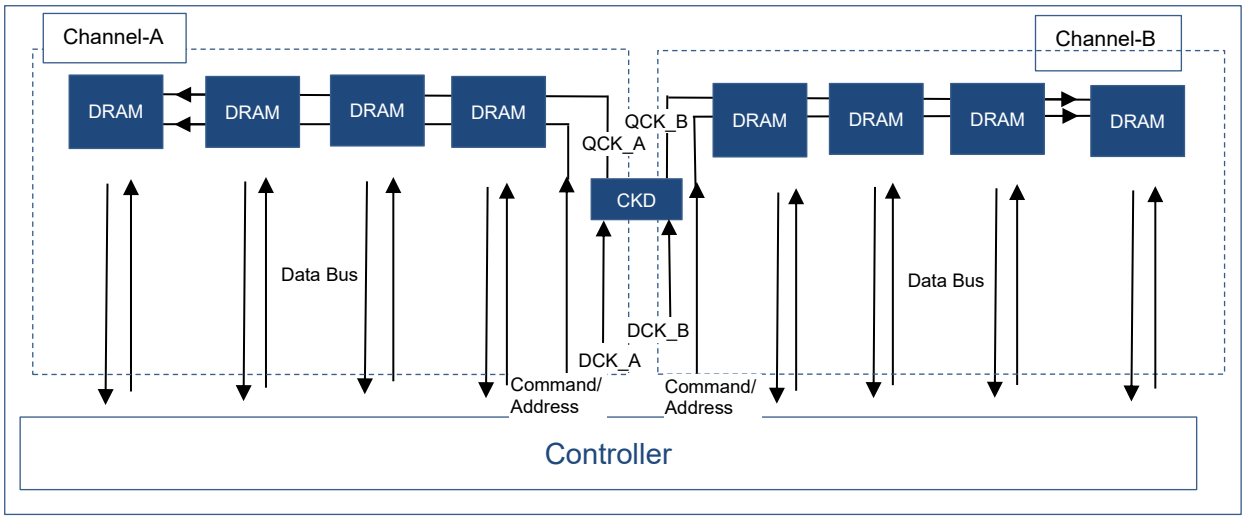


Figure 7 — Fly-by Topology Example

6.7.2 Lead-in versus Loaded Sections

The CK, CMD/ADR, and CS topologies are conceptually divided into two topology sections. For CMD/ADR and CS, the segments between the connector and the first SDRAM node via (TL0 + TL1) are collectively termed the lead-in section.

For CK, TL0 is same as DCK while TL1 is the same as QCK. The CKD is considered transparent from a length calculation standpoint, so the total lead-in section includes DCK + QCK.

The segments that run between SDRAM node vias (TL3), as well as the SDRAM load stubs (TL2), are collectively termed the loaded section.

To reduce the impedance discontinuity seen at the first load, the lead-in section is routed at a lower nominal impedance than the loaded section, although some modules may vary. The transition from the wider lead-in trace width to the standard width of the loaded section must occur within a length window preceding the first SDRAM node via.

The two different impedance sections at lead-in may not be required for example for the modules which have short TL0+TL1 length (e.g., less than 25 mm). This should be determined by simulation.

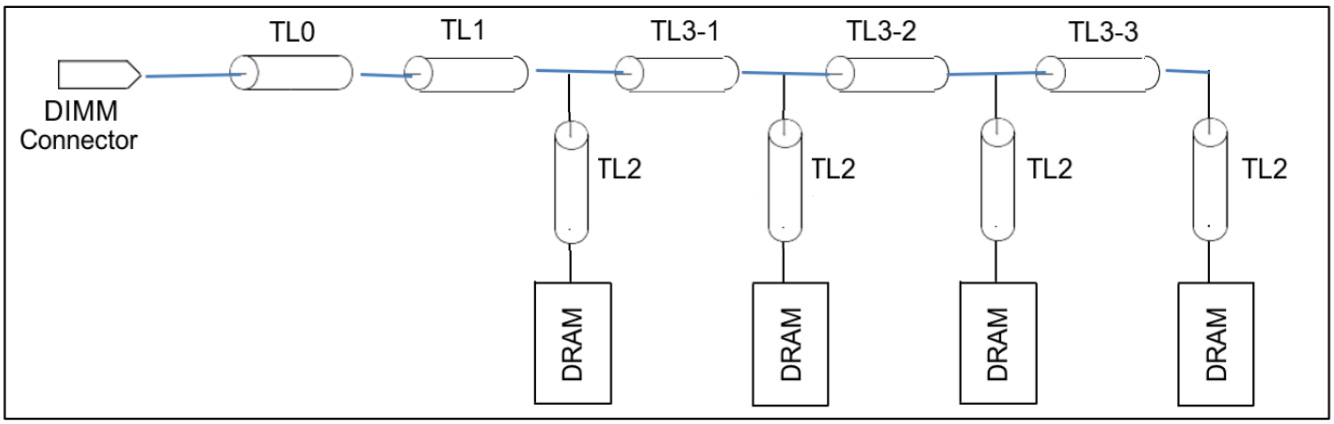


Figure 8 — Command/Address Routing Topology Example

6.7.3 Length/Delay Matching to SDRAM Devices

As mentioned previously, length/delay matching is required between the connector and each SDRAM individually. The length/delay matching process is iterative in nature, and there is no single-best method defined. It is generally recommended that the path from the connector to the first SDRAM (TL0 + TL1) be matched across the CK group, and then across the CTRL and ADD/CMD groups—as per the length matching guidelines—adjusting the CK length as needed to reach the length window of the CTRL and ADD/CMD groups. For the DDR5 CAMM2, usually the breakout via from the DRAM pin is located between 4 DRAM pins and lengths are all 0.6mm, in that case TL2 does not need to be included in the length calculation. If signal group (Addr, CS, CK) TL2 lengths are not the same, then length adjustment may be needed to align timing further down the daisy-chain. When CK has 1 load and Address bits have two loads, prop delay is normally compensated in the stripline length but may need other length adjustments to align timing.

Once length/delay matching to the first device is complete, the length matching to the remaining devices is straightforward and can be accomplished by simply length-matching the intra-node segments (TL3-x), assuming the TL2 stub length does not vary between signal groups, or from SDRAM to SDRAM.

6.7.3 Length/Delay Matching to SDRAM Devices (cont'd)

The total compensated length from the CAMM2 pin to the first and last SDRAM is documented in the segment length tables for each module type, in the Annex net structure definitions sections; however, it is assumed that the length matching rules are met at all SDRAM devices inclusive of velocity compensation.

Since the lead-in section can have a wide variation in the proportion of its length routed as microstrip (MS) and stripline (SL), the length/delay matching process includes a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the stripline equivalent length. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

6.7.4 Load/Delay Compensation

The concept of load/delay compensation refers to the technique whereby the segment lengths between SDRAMS, on the CK and CS signal groups, are purposely lengthened to add additional flight time delay, as required to compensate for the fact that the CMD/ADR topology for 2 rank modules has 2 loads (1 top + 1 bottom) for each fly-by node, whereas the CK and CS topologies have only one load per node. Where implemented, the CK and CS segments between SDRAMs shall be routed longer than the corresponding segment on CMD/ADR group. A specific number can be identified using simulation or calculation. The net result of this compensation is less overall CMD/ADR to CK skew across the module, thereby improving the ability of the controller to correctly center the CK within the CMD/ADR valid window at each SDRAM.

6.7.5 ALERT_n Wiring

Wiring example for the ALERT_n signal. DDR5 CAMM2 has 2 channels of signal groups, but there is one ALERT_n per channel. For each channel, ALERT is daisy-chained across the DRAM in any order across the subchannels. The connection order can be the same as clock or can be reverse order of clock. It requires a termination resistor at the far end from the CAMM2 connector pin.

6.7.5 ALERT_n Wiring (cont'd)

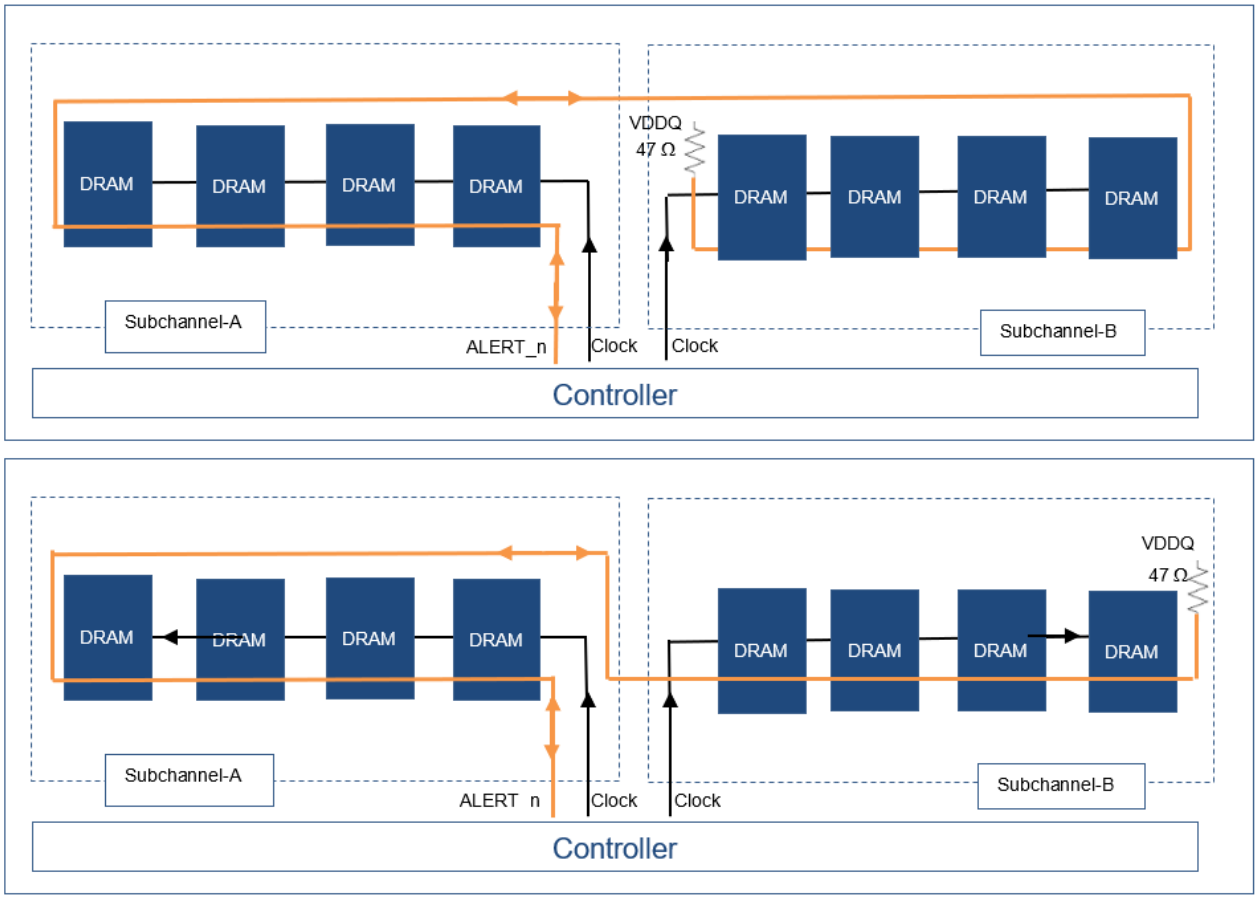


Figure 9 — ALERT_n Wiring Examples

6.7.6 RESET_n Wiring

Figure 10 is a wiring example for the DDR5 CAMM2 RESET_n signal. The topology should be a daisy chain. There is no restriction on the connection ordering. There is one RESET_n per channel. For each channel, RESET_n is daisy-chained across the DRAM in any order across the subchannels.

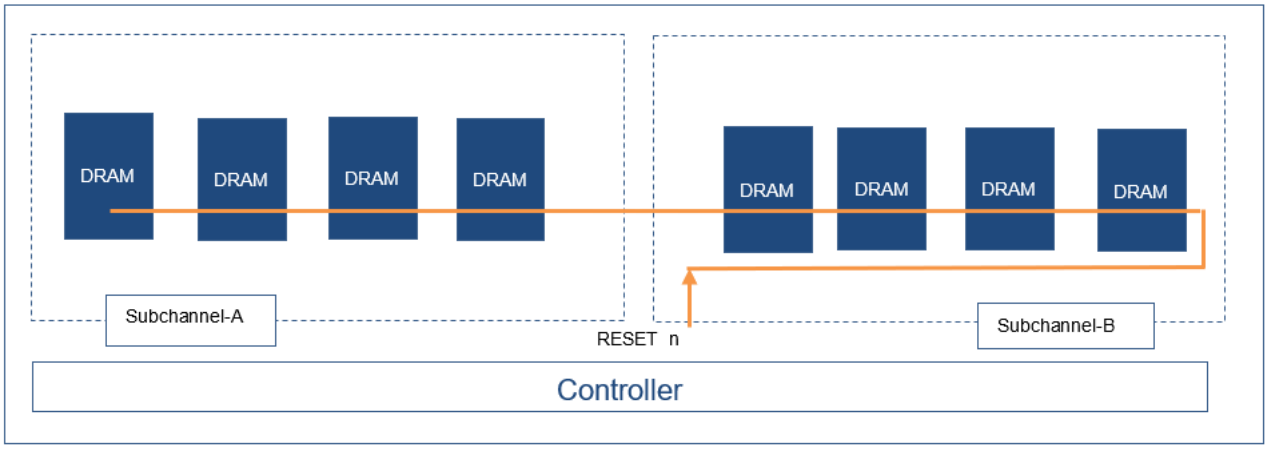


Figure 10 — RESET_n Wiring Example

For LP5 CAMM2 designs, the RESET_n signal follows the same principles as above with a daisy-chain pattern from the CAMM2 connector pin through the LP5 packages.

6.7.7 Via Compensation

The CAMM2 reference designs add the vertical length that the signal travels along the via barrel to the length calculation.

For the DRAMs which share a via (2 rank module case), the via barrel lengths to the top and bottom DRAMs are different. In that case the via barrel lengths are not included in the length calculation. Please see the length file which is zipped with the reference design

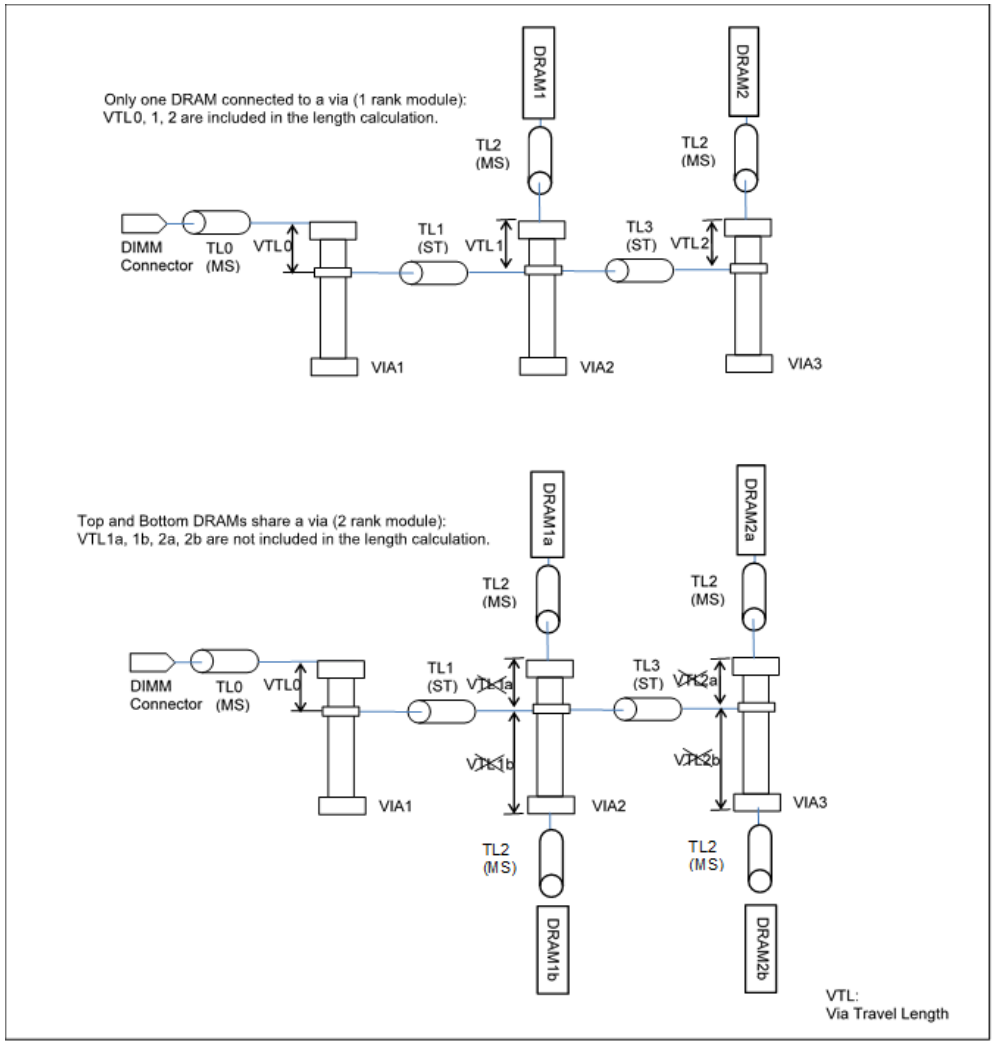


Figure 11 — Via Compensation Explanation

6.7.8 Plane Referencing

Table 22 — Plane Referencing for DDR5 and LP5

Signals	Reference	Notes
DQ, DQS, DM	Ground	
Command/Address	Ground	
Chip Select	Ground	
Clock, WCK	Ground	
Sideband Bus	Ground	

6.8 Address Mirroring

DDR5 SDRAM has MIR input pin. This pin is connected to VSS or VDDQ on the PCB. This pin is used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSS if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1), CA4 with CA5 (not CA3).

The common use case is placing two DDR5 SDRAMs at the same X-Y location on top and bottom sides of the PCB, and then strapping the MIR pin to VSS/VDDQ. The use case purpose is to reduce the distance between the same number CA and reduce the stub trace length.

Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected to VDDQ.

If MIR is employed, the CA12 pin of DRAM (which is now changed to CA13 by MIR) needs to be tied to VDDQ.

The MIR pin configuration is documented in the checklist, which is zipped with the reference design, and the Annex Specification will identify how MIR is used.

6.9 CAMM2 Routing Space Constraints

These design rules are intended to be used for the reference CAMM2 designs submitted to JEDEC for ballot.

When rules which are not defined here are used, it should be noted in the annex for each specific raw card.

These rules are for design of the reference card only. It is not required that these rules be met by individual manufacturers building from the reference designs.

CAMM2s manufactured from the reference designs may use modified rules to support their manufacturing process.

Table 23 — Routing Space Constraints

	Category	Item	Constraint Value (mm)	Note
1	Via	Drill/Pad/Anti-pad / Soldermask	0.20/0.40/0.60/ Soldermask feature may vary depending on designer preference.	One example is setting the soldermask equal to the pad and allowing the PCB shop to adjust as required. Rule may be different between SMD and non-SMD.
2	Micro-via (outer/Inner layer)	Drill/Pad/Anti-pad / Soldermask	0.10/0.25/0.55 0.10/0.25/0.42	Better practice Spec Limit
3	Micro-via	Stacking	Allowed	Not over buried via
4	Micro-via	Via in Pad	Allowed	Allowed in DRAM pad, not allowed in CAMM2 pad
5	Buried via	Drill/Pad/Anti-pad / Soldermask	0.20/0.40/0.60	Filled, cap plating not required
6	Spacing	copper to copper (Outer/Inner)	0.075 / 0.070	Depends on Cu thickness
7	Spacing	Pad to pad (For pads of different components that are soldered down.)	0.200	
8	Spacing	Line to (N)SMD pad (12 V / the others)	0.113 / 0.100	Depends on Cu thickness on outer layer
9	Spacing	Line to line (Single / Differential pair)	0.100 / 0.090	Depends on whether inner or outer layer routing and Cu thickness
10	Spacing	Line to shape	0.125	Where impedance is important, use the 0.20 rule. Depends on whether inner or outer layer routing.
11	Spacing	Shape to shape	0.100	
12	Spacing	Via(pad) to NSMD pad (12 V / the others / same Net)	0.113 / 0.100 / 0.100	
13	Spacing	Via(pad) to SMD pad (12 V / the others / same Net)	0.113 / 0.100 / 0.020	

Table 23 — Routing Space Constraints (cont'd)

	Category	Item	Constraint Value (mm)	Note
14	Spacing	Via(pad) to Via(pad)	0.125	
15	Spacing	Via(pad) to Line (Outer/Inner)	0.09 / 0.07	
16	Spacing	Micro-via pad to Line (outer)	0.125 / 0.100	Better / Spec Limit
17	Spacing	Micro-via pad to Line (inner)	0.125 / 0.083	Better / Spec Limit
18	Spacing	Micro-via pad to Micro-via pad (Same net)	0	
19	Spacing	Micro-via pad to Micro-via pad (Different net)	0.125 / 0.090	
20	Spacing	Micro-via pad to Buried via or Through Hole via pad (same net)	0	
21	Spacing	Micro-via pad to Buried via or Through Hole via pad (Different net – outer)	0.275 / 0.124	Better / Spec Limit
22	Spacing	Micro-via pad to Buried via or Through Hole via pad (Different net – inner)	0.275 / 0.100	Better / Spec Limit
23	Spacing	Drill wall to Board edge (nominal)	0.450	Nominal board edge and drill being centered in pad
24	Comp to Comp	IC to IC (max. PKG size)	0.250	Inductor is assumed IC. (Max PKG size 4.3 mm)
25	Comp to Comp	IC (max.) to Passive (nominal)	0.250	
26	Comp to Comp	Passive to Passive (nominal PKG size)	0.250	
27	Copper keepout	Board top edge (nom.) to copper	0.250	

6.10 CAMM2 Physical Requirements

6.10.1 Via Placement

Signal Vias must not be placed close together (except differential signals) to reduce crosstalk. Recommended to place power or GND Via between Signal Vias.

Vias for different channels must be spaced 2mm apart to reduce channel-to-channel crosstalk.

6.10.2 Component Pad Sizes and Geometry

Pads for components are left to the reference card designer to define.

Manufacturers of these CAMM2 reference designs may adjust pad sizes and geometry.

6.10.3 Unused CK, CS Termination

For 1 Rank, Unused DDR5 CK should be terminated with two 33ohm resistors to VDDQ (single ended termination)

Systems that do not support CS2/3 for LP5 CAMMs should terminate CS2/3 on the motherboard to VDD2 or equivalent 1.05 V source.

If using a Clock Driver device, all SoC clock pairs are routed to the clock driver and the clock driver shall terminate the unused clocks to VSS.

6.10.4 DQ/CA Stub Resistor

No DQ, Command/address stub resistor for all CAMM2s.

6.10.5 ZQ Calibration Wiring

The DDR5 SDRAMs and clock driver have a ZQ pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All CAMM2s must connect a 240 Ω ± 1% resistor from this pin of the SDRAM to ground (VSS). Every SDRAM package must have its own ZQ resistor. Sharing is not allowed.

The LP5 ZQ pin is terminated through a 240 Ω ± 1% resistor to VDDQ.

6.10.6 TEN Wiring

TEN is a test enable pin on the DDR5 SDRAMs. It is not intended to be used on CAMM2s. It must be tied low VSS at each SDRAM.

6.10.7 Loop Back Wiring

DDR5 CAMM2s do not have Loopback signal connectivity to the connector pins. However, Loopback functionality is useful for module debug, so at the initial design Loop Back signals are connected to the test pads on the modules. The topology should be a daisy chain. The test pads are required for each channels A and B. On the production designs, test pads can be removed.

6.10.8 MIR Wiring

With the MIR pin connected to VDDQ, the DDR5 SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSSQ if no CA mirror is required. The MIR pin connection information may be found in each Reference Design package.

6.10.9 CA_ODT Wiring

For the DDR5 CAMM2, usually only the CA_ODT pin for the DDR5 SDRAM at the end of fly-by is connected to VDDQ. The CA_ODT pin connection information may be found in each Reference Design package.

6.10.10 CAI Wiring

With the CAI pin connected to VDDQ, DDR5 SDRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSS if no CA inversion is required.

Usually, DDR5 CAMM2s do not need an inversion pin. The CAI pin cannot be left floating, it must be connected to VSS on the DDR5 CAMM2.

6.11 Reference Stackups

The section defines the preferred stackup for 8-, 10-, 12, and 14-layer CAMM2s. Stackup for specific cards may be different from the suggested stackup in the tables below.

Multiple factors influence module stackup definition, and it is expected that module vendors will define their stackup in conjunction with PCB vendors, based on many factors including material properties, material availability, electrical performance, and cost. The stackups shown here are intended for reference only, to demonstrate feasibility of the key performance.

The actual layer construction, trace widths and target impedances used for the design and simulation are documented in each annex.

6.11.1 Reference 10-Layer DDR5 and LP5 CAMM2 Stackup

										DDR	DQ, CA, CS	CK		DQS
										LPDDR	DQ, CA, CS		WCK	CK, DQS
	Routing Layer	Description	Cu	Material Design	Df	Dk 1 GHz	Thickness (mil)	Thickness (um)	Thickness (mm)	40 ± 5 ohm single-end	45 ± 7 ohm Differential	65 ± 7 ohm Differential	75 ± 7 ohm Differential
		Solder Mask			0.047		0.50	12.70	0.01				
TOP	1	Break out /VDD	0.5 oz + plating	MS			2.07	52.58	0.05	4.6 Mil (.11684mm)	10.6/4 Mil	5.6/4 Mil	4.5/5 Mil (.1143/.127mm)
		Prepreg		106 (HRC, 75%)	0.022	3.52	2.08	52.83	0.05	40.42 Ohm	46.35 Ohm	65.59 Ohm	74.51 Ohm
	2	Gnd	1 oz				1.25	31.75	0.03				
		Core		1086*1	0.0171	3.82	3.00	76.20	0.08				
IN1	3	Signal	0.5 oz	SL			0.66	16.76	0.02	4 Mil (.1016mm)	8.5/4 Mil	5/4 Mil	4/4 Mil (.1016/.1016mm)
		Prepreg		1080*1 (MRC, 65%)	0.0209	3.68	2.41	61.21	0.06	39.71 Ohm	45.79 Ohm	65.34 Ohm	75.66 Ohm
	4	Gnd	1 oz				1.25	31.75	0.03				
		Core		1086*1	0.0171	3.82	3.00	76.20	0.08	40.02 (40.49) Ohm	45.79 Ohm	65.08 Ohm	75.22 Ohm
IN2	5	Signal	1 oz	SL/DSL			1.25	31.75	0.03	L5/L6 SL 4.1 (4) Mil (.10414 -.1016mm)	9.4/4 Mil	5.2/4 Mil	L5/L6 SL 4/5 Mil (.1016 /.127mm)
		Prepreg					20.00	508.00	0.51				
IN3	6	Signal	1 oz	SL/DSL			1.25	31.75	0.03	L5/L6 DSL 5.4 Mil (.13716 mm)	9.4/4 Mil	5.2/4 Mil	L5/L6 DSL 4.2/4 Mil (.10668/.1016)
		Core		1086*1	0.0171	3.82	3.00	76.20	0.08	39.86 Ohm	45.79 Ohm	65.08 Ohm	75.08 Ohm
	7	Gnd	1 oz				1.25	31.75	0.03				
		Prepreg		1080*1 (MRC, 65%)	0.0209	3.68	2.41	61.21	0.06				
IN4	8	Signal	0.5 oz	SL			0.66	16.76	0.02	4 Mil (.1016 mm)	8.5/4 Mil	5/4 Mil	4/4 Mil (.1016 /.1016 mm)
		Core		1086*1	0.0171	3.82	3.00	76.20	0.08	39.71 Ohm	45.79 Ohm	65.34 Ohm	75.66 Ohm
	9	Gnd	1 oz				1.25	31.75	0.03				
		Prepreg		106 (HRC, 75%)	0.022	3.52	2.09	53.09	0.05				
BOT	10	Break out/VDDQ	0.5 oz + plating	MS			2.07	52.58	0.05	4.6 Mil (.11684 mm)	10.6/4 Mil	5.6/4 Mil	4.5/5 Mil (.1143 / .127mm)
		Solder Mask			0.047		0.50	12.70	0.01	40.42 Ohm	46.48 Ohm	65.73 Ohm	74.51 Ohm
				Total			54.95	1395.73	1.40				

6.11.2 Reference 12-Layer DDR5 CAMM2 Stackup

										DDR	DQ, CA, CS	CK	DQS
	Routing Layer	Description	Cu	Material Design	Df	Dk 1 GHz	Thickness (mil)	Thickness (um)	Thickness (mm)	40 ± 5 ohm single-end	45 ± 7 ohm Differential	75 ± 7 ohm Differential
		Solder Mask			0.047		0.50	12.70	0.01			
TOP	1	Break out /VDD		MS			1.60	40.64	0.04	4.6/4 Mil (.11684 mm /.1016 mm)	10.5/4 Mil	4.5/5 Mil (.1143/ .127 mm)
		Prepreg		106	0.022	3.52	1.94	49.28	0.05	40.42 Ohm	46.29 Ohm	74.51 Ohm
GND1	2	Gnd		Gnd/Pwr			1.30	33.02	0.03			
		Core		2112*1	0.0171	3.82	3.00	76.20	0.08			
IN1	3	Signal		SL			0.65	16.51	0.02	4/4 Mil (.1016mm/.1016 mm)	9.4/4 Mil	4.2/4 Mil (.10668 /.1016 mm)
		Prepreg		1080*1	0.0209	3.68	2.80	71.12	0.07	39.71 Ohm	44.97 Ohm	75.66 Ohm
GND2	4	Gnd		Gnd/Pwr			1.30	33.02	0.03			
		Core		2112*1	0.0171	3.82	3.00	76.20	0.08	39.71 Ohm	44.97 Ohm	75.66 Ohm
IN2	5	Signal		SL			0.65	16.51	0.02	4 Mil (.1016 mm)	9.4/4 Mil	4.2/4 Mil (.10668 / .1016 mm)
		Prepreg		1080*1	0.0209	3.68	2.80	71.12	0.07			
VCC1	6	VDD/VDDQ		Gnd/Pwr			1.30	33.02	0.03			
		Prepreg		2112*1	0.0171		15.00	381.00	0.38			
VCC2	7	VDD/VDDQ		Gnd/Pwr			1.30	33.02	0.03			
		Prepreg		1080*1	0.0209	3.68	2.80	71.12	0.07	39.71 Ohm	44.97 Ohm	75.66 Ohm
IN3	8	Signal		SL			0.65	16.51	0.02	4/4 Mil (.1016mm/.1016 mm)	9.4/4 Mil	4.2/4 Mil (.10668/ .1016 mm)
		Core		2112*1	0.0171	3.82	3.00	76.20	0.08	40.02 (40.49) Ohm		75.22 Ohm
GND3	9	Gnd		Gnd/Pwr			1.30	33.02	0.03			
		Prepreg		1080*1	0.0209	3.68	2.80	71.12	0.07	39.71 Ohm	44.97 Ohm	75.66 Ohm
IN4	10	Signal		SL			0.65	16.51	0.02	4/4 Mil (.1016mm/.1016 mm)	9.4/4 Mil	4.2/4 Mil (.10668/ .1016 mm)
		Core		2112*1	0.0171	3.82	3.00	76.20	0.08			
GND4	11	Gnd		Gnd/Pwr			1.30	33.02	0.03			
		Prepreg		106	0.022	3.52	1.94	49.28	0.05			
BOT	12	Break out/VDDQ		MS			1.60	40.64	0.04	5.6/4 Mil (.14224/.1016 mm)	10.5/4 Mil	4.5/5 Mil (.1143/ .127 mm)
		Solder Mask			0.047		0.50	12.70	0.01	40.42 Ohm	46.29 Ohm	74.51 Ohm
				Total			55.12	1400.05	1.40			

6.11.3 Reference 14-Layer DDR5 CAMM2 Stackup

									DDR	DQ, CA, CS	CK	DQS
	Routing Layer	Description	Cu	Material Design	Df	Dk 1 GHz	Thickness (mil)	Thickness (um)	Thickness (mm)	40 ± 5 ohm single-end	45 ± 7 ohm Differential	75 ± 7 ohm Differential
		Solder Mask			0.047		0.50	12.70	0.01			
TOP	1	Break out/VDD	0.5 oz+ plating	MS			1.88	47.75	0.05	4.6 Mil (.11684mm)	10.5/4 Mil	4.5/5 Mil (.1143/.127mm)
		Prepreg		106(HRC,74 %)	0.022	3.79	2.06	52.32	0.05	40.42 Ohm	45.69 Ohm	74.51 Ohm
GND1	2	Gnd	1 oz				1.25	31.75	0.03			
		Core		1080*1	0.0171	4.06	3.00	76.20	0.08			
IN1	3	Signal	0.5 oz	SL			0.66	16.76	0.02	4 Mil (.1016mm)	8.8/4 Mil	4/4 Mil (.1016/.1016mm)
		Prepreg		1080 (MRC,67%)	0.0209	3.98	2.75	69.85	0.07	39.71 Ohm	45.24 Ohm	75.66 Ohm
GND2	4	Gnd	1 oz				1.25	31.75	0.03			
		Core		1080*1	0.0171	4.06	3.00	76.20	0.08			
IN2	5	Signal	0.5 oz	SL			0.66	16.76	0.02	4 Mil (.1016mm)	8.8/4 Mil	4/4 Mil (.1016/.1016mm)
		Prepreg		1080(MRC,67 %)	0.0209	3.98	2.73	69.34	0.07	39.71 Ohm	45.13 Ohm	75.66 Ohm
GND3	6	Gnd	1 oz				1.25	31.75	0.03			
		Core		1080*1	0.0171	4.06	3.00	76.20	0.08	40.02 (40.49) Ohm	46.17 Ohm	75.22 Ohm
IN3	7	Signal	1 oz	SL/DSL			1.25	31.75	0.03	L5/L6 SL 4.1 (4) Mil (.10414 -.1016mm)	9.2/4 Mil	L5/L6 SL 4/5 Mil (.1016/.127mm)
		Prepreg		2116(MRC,55 %)	0.0176	4.31	6.00	152.40	0.15			
IN4	8	Signal	1 oz	SL/DSL			1.25	31.75	0.03	L5/L6 DSL 5.4 Mil (.13716mm)	9.2/4 Mil	L5/L6 DSL 4.2/4 Mil (.10668/.1016)
		Core		1080*1	0.0171	4.06	3.00	76.20	0.08	39.86 Ohm	46.17 Ohm	75.08 Ohm
GND4	9	Gnd	1 oz				1.25	31.75	0.03			
		Prepreg		1080(MRC,67 %)	0.0209	3.98	2.70	68.58	0.07			
IN5	10	Signal	0.5 oz	SL			0.66	16.76	0.02	4 Mil (.1016mm)	8.8/4 Mil	4/4 Mil (.1016/.1016mm)
		Core		1080*1	0.0171	4.06	3.00	76.20	0.08	39.71 Ohm	44.95 Ohm	75.66 Ohm
GND5	11	Gnd	1 oz				1.25	31.75	0.03			
		Prepreg		1080(MRC,67 %)	0.0209	3.98	2.71	68.83	0.07			
IN6	12	Signal	0.5 oz	SL			0.66	16.76	0.02	4 Mil (.1016mm)	8.8/4 Mil	4/4 Mil (.1016/.1016mm)
		Core		1080*1	0.0171	4.06	3.00	76.20	0.08	39.71 Ohm	45.02 Ohm	75.66 Ohm
GND6	13	Gnd	1 oz				1.25	31.75	0.03			
		Prepreg		106(HRC,74 %)	0.022	3.79	2.06	52.32	0.05			
BOT	14	Break out/VDDQ	0.5 oz+plating	MS			1.88	47.75	0.05	4.6 Mil (.11684mm)	10.5/4 Mil	4.5/5 Mil (.1143/.127mm)
		Solder Mask			0.047		0.50	12.70	0.01	40.42 Ohm	45.69 Ohm	74.51 Ohm
				Total			55.16	1401.06	1.40			

6.11.4 Reference 16-Layer DDR5 CAMM2 Stackup

										DDR	DQ, CA, CS	CK	DQS
	Routing Layer	Description	Cu	Material Design	Df	Dk 1 GHz	Thickness (mil)	Thickness (um)	Thickness (mm)	40 ± 5 ohm single-end	45 ± 7 ohm Differential	75 ± 7 ohm Differential
		Solder Mask			0.047		0.50	12.70	0.01	4.7 Mil 41.05 ohms	11/4 mils 44.93 Ohm	4.8/5 mils 74.39 Ohm
TOP	1	Break out/VDD	0.5 oz + plating	MS			1.60	40.64	0.04			
		Prepreg			0.022	3.52	1.94	49.28	0.05			
GND1	2	Gnd	1 oz				1.25	31.75	0.03			
		Core		2112*1	0.0171	3.83	2.50	63.50	0.06	3.5 Mil 39.27 ohms	8/4 Mil 44.35 ohms	3.5/4 Mil 75.87 ohms
IN1	3	Signal	0.5 oz	SL			0.66	16.76	0.02			
		Prepreg			0.0209	3.68	2.30	58.42	0.06			
GND2	4	Gnd	1 oz				1.25	31.75	0.03			
		Core		2112*1	0.0171	3.83	2.50	63.50	0.06	3.7 mils 38.97 ohms	8/4 Mil 45.65 ohms	3.7/4 Mil 75.11 ohms
IN2	5	Signal	0.5 oz	SL			0.66	16.76	0.02			
		Prepreg			0.0209	3.68	2.50	63.50	0.06			
GND3	6	Gnd	1 oz				1.25	31.75	0.03			
		Core		2112*1	0.0171	3.83	2.50	63.50	0.06	3.5/5 mils 38.58 ohms	7.5/4 Mil 46.77 ohms	3.5/5 Mil 74.32 ohms
IN3	7	Signal	1 oz	SL			1.25	31.75	0.03			
		Prepreg			0.0209	3.68	2.80	71.12	0.07			
VCC1	8	VCC/Gnd	1 oz				1.25	31.75	0.03			
		Prepreg			0.022	3.52	1.88	47.75	0.05			
VCC2	9	VCC/Gnd	1 oz				1.25	31.75	0.03			
		Prepreg			0.0209	3.68	2.80	71.12	0.07	3.5/5 mils 38.58 ohms	7.5/4 Mil 46.77 ohms	3.5/5 Mil 74.32 ohms
IN4	10	Signal	1 oz	SL			1.25	31.75	0.03			
		Core		2112*1	0.0171	3.83	2.50	63.50	0.06			
GND4	11	Gnd	1 oz				1.25	31.75	0.03			
		Prepreg			0.0209	3.68	2.50	63.50	0.06	3.7 mils 38.97 ohms	8/4 Mil 45.65 ohms	3.7/4 Mil 75.11 ohms
IN5	12	Signal	0.5 oz	SL			0.66	16.76	0.02			
		Core		2112*1	0.0171	3.83	2.50	63.50	0.06			
GND5	13	Gnd	1 oz				1.25	31.75	0.03			
		Prepreg			0.0209	3.68	2.30	58.42	0.06	3.5 Mil 39.27 ohms	8/4 Mil 44.35 ohms	3.5/4 Mil 75.87 ohms
IN6	14	Signal	0.5 oz	SL			0.66	16.76	0.02			
		Core		2112*1	0.0171	3.83	2.50	63.50	0.06			
GND6	15	Gnd	1 oz				1.25	31.75	0.03			
		Prepreg			0.022	3.52	1.94	49.28	0.05	4.7 mils 41.05 ohms	11/4 mils 44.93 Ohm	4.8/5 Mil 74.39 ohms
BOTTOM	16	Break out/VDDQ	0.5 oz + plating	MS			1.60	40.64	0.04			
		Solder Mask			0.047		0.50	12.70	0.01			
				Total			55.30	1404.62	1.40			

6.12 Module Sideband Bus

Please refer to the latest version of the JESD403-1: JEDEC Module Sideband Bus(Sideband Bus).

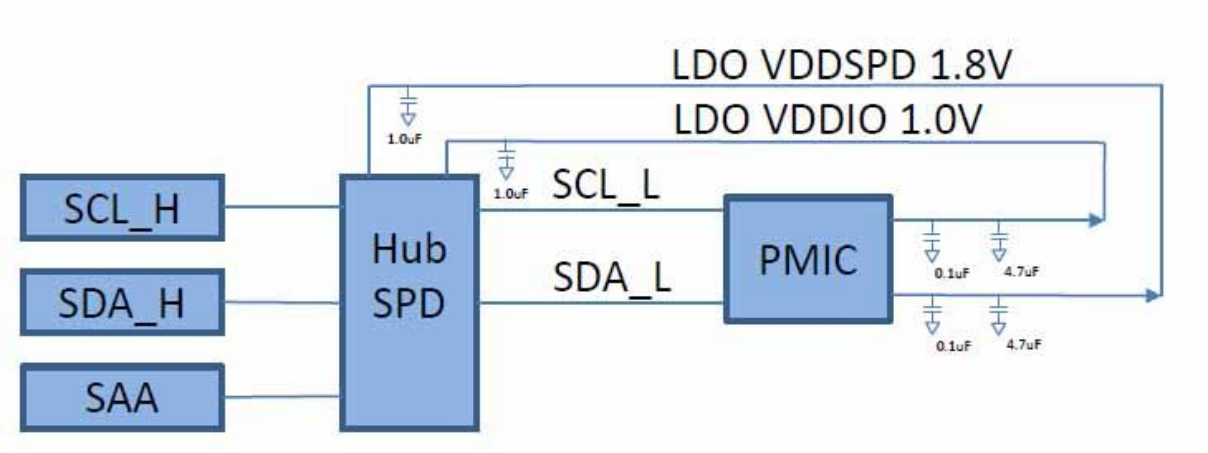


Figure 12 — Sideband Bus Wiring Example

6.13 Bit Swizzling Rules

All CAMM2 designs must follow the DQ mapping of the JEDEC Reference CAMM2 Design of the same configuration. For example, newly designed 1Rx16 CAMM2 must follow the DQ mapping of approved 1Rx16 JEDEC DDR5 CAMM2 reference design. Likewise, a newer version of LP5 CAMM2, like Raw Card E1, must follow the DQ mapping of the original design, E0.

DDR5 modules do not need to record DQ mapping in SPD but need to follow the following bit swizzling rules.

Rule 1: Bits within a nibble + strobe pair must stay together

Rule 2: Nibbles may be swapped within the same byte

Rule 3: Definition of mapping is for rank 0 only. All even ranks have the same DQ mapping.

Even rank to odd rank mapping is to swap bit 0 with bit 1, swap bit 2 with bit 3, swap bit 4 with bit 5 and swap bit 6 with bit 7

The DDR5 CAMM2 design should follow the DQ mapping of the JEDEC Reference CAMM2 Design of the same configuration. For example, newly designed 1Rx16 CAMM2 should follow the DQ mapping of approved 1Rx16 JEDEC DDR5 CAMM2 Reference design.

The LP5 modules must follow the following bit swizzling rules.

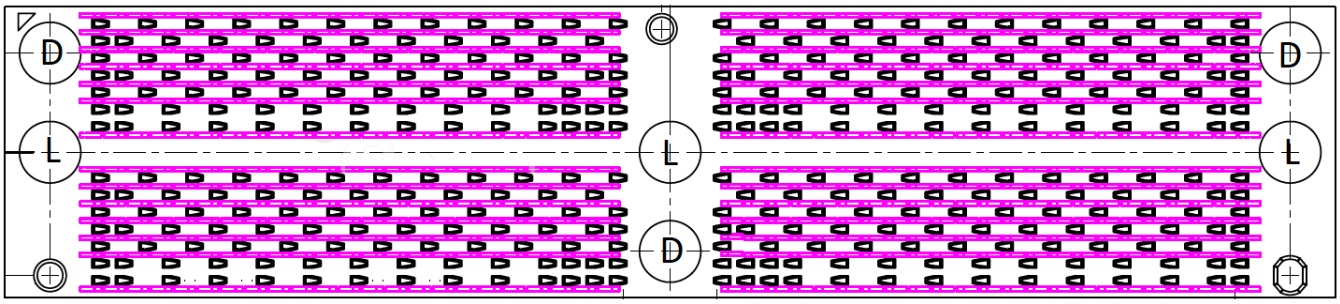
Rule 1: Bits may be swapped within the same byte

6.14 Informative: CAMM2 Mounting

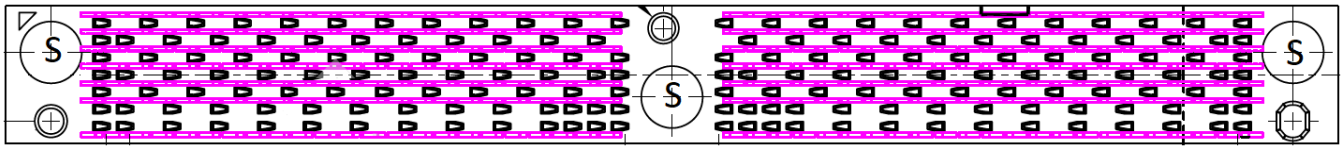
This section is informative only and contains no new CAMM2 requirements. It is provided to address common mounting questions between Main Boards, CAMM2 connectors, and modules.

JEDEC JC11 defines the CAMM2 connector mechanical requirements. For mounting, several mounting holes and alignment posts are provided.

- For the dual-channel version (Variation AXXX, CXXX, DXXX), three mounting holes are provided for:
  - DDR5 DC CAMM2's (denoted by "D" below)
  - LP5 CAMM2's (denoted by "L" below)



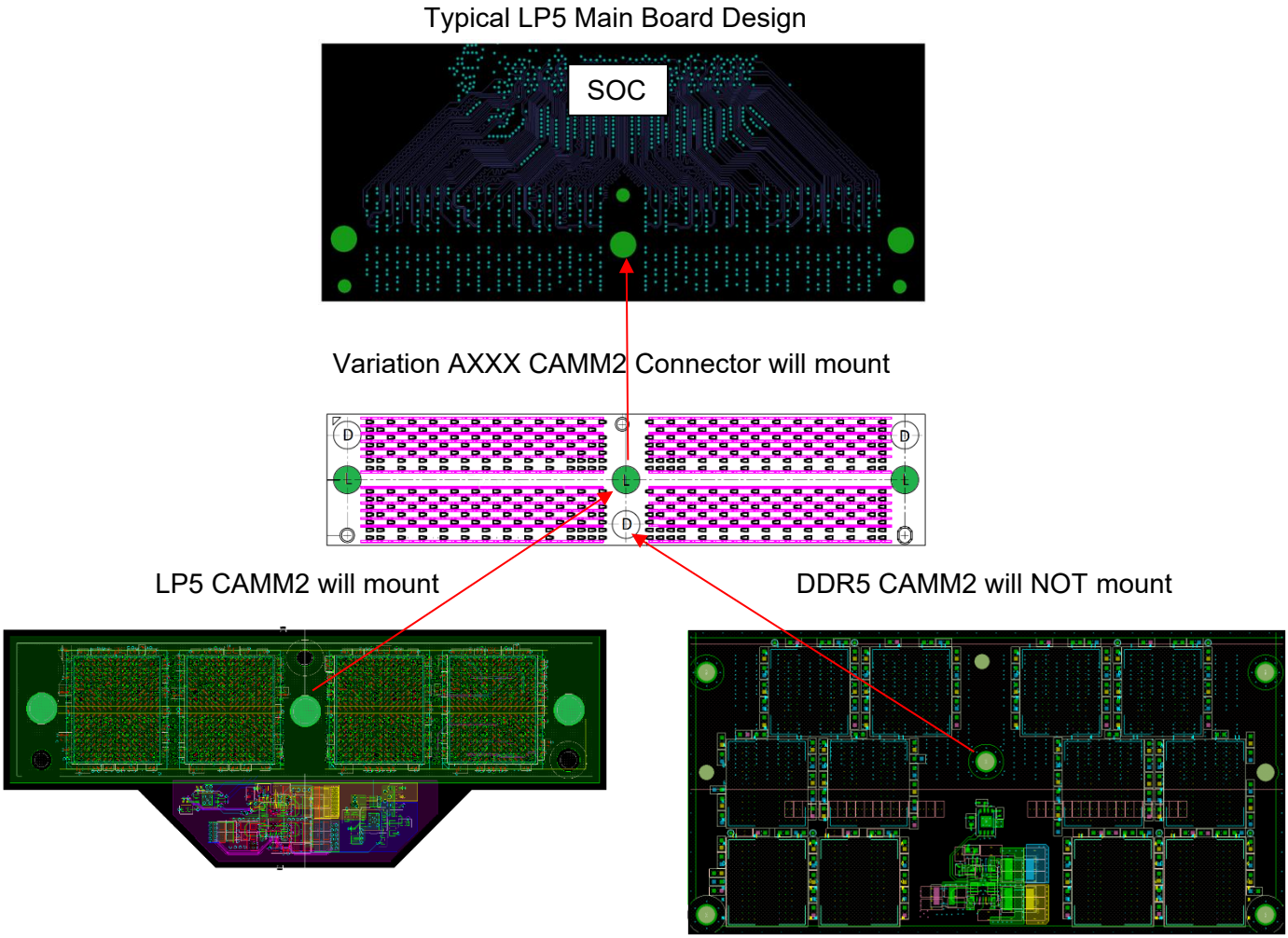
- For the single-channel version (Variation BXXX), three mounting holes are provided for:
  - DDR5 SC CAMM2's (denoted by "S" below)



The CAMM2 raw cards have corresponding mounting holes that match the above assignments.

The Main Board (MB) designs also have corresponding mounting holes. The LP5 CAMM2 MBs are intuitive while the DDR5 MBs require some explanation.

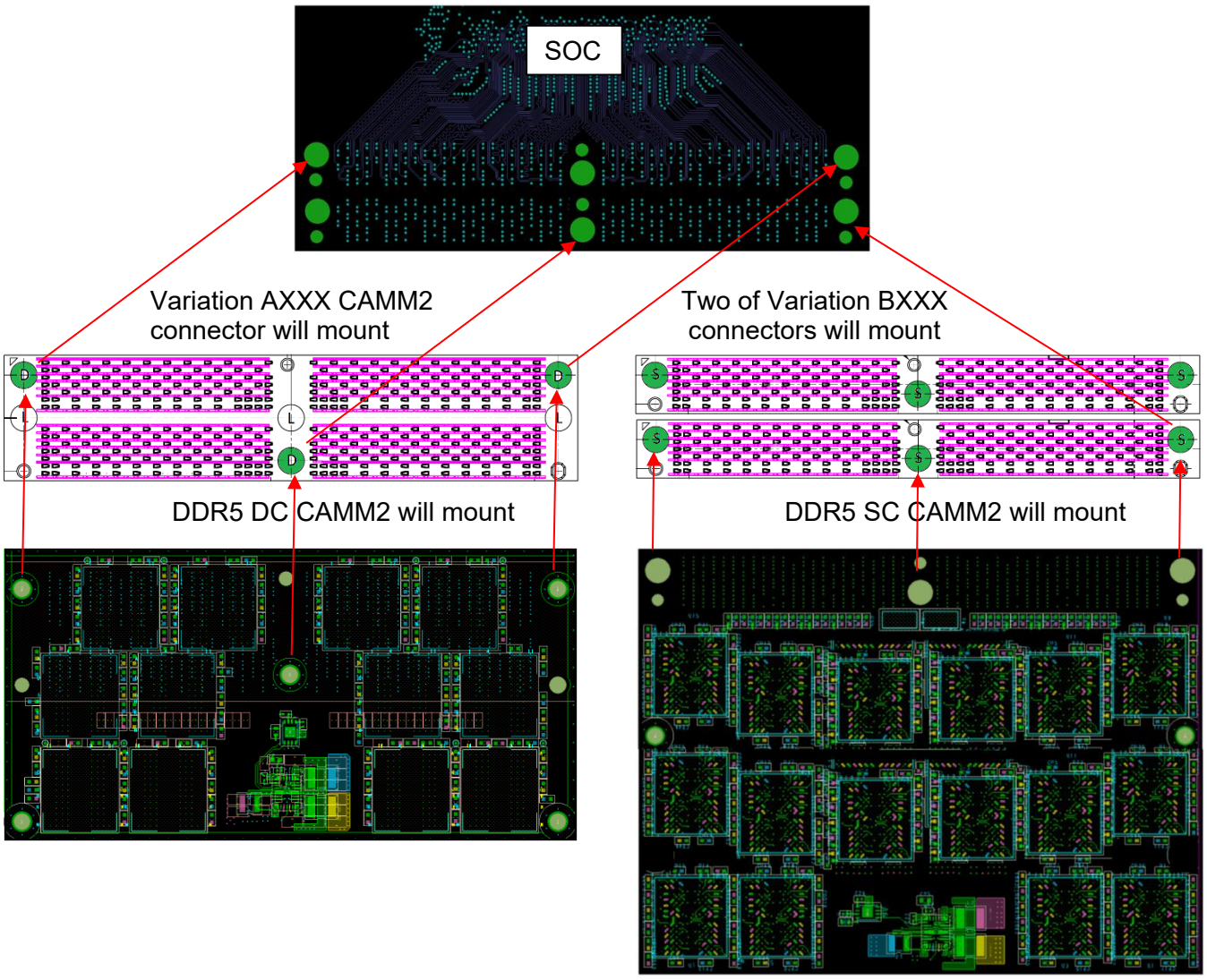
6.14 Informative: CAMM2 Mounting (cont'd)



The LP5 CAMM2, connector and MB design have mounting holes that align. The "D" mounting holes of the connector do not have corresponding MB mounting holes, so there is no mechanism to attach the DDR5 CAMM2 to this motherboard. This is intentional as LP5 CAMM2 MBs do not support DDR5 modules.

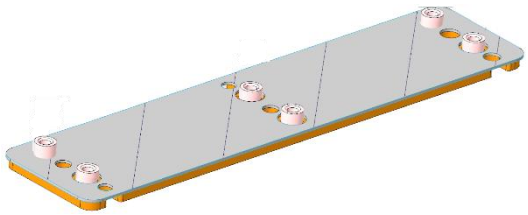
6.14 Informative: CAMM2 Mounting (cont'd)

Typical DDR5 Main Board Design



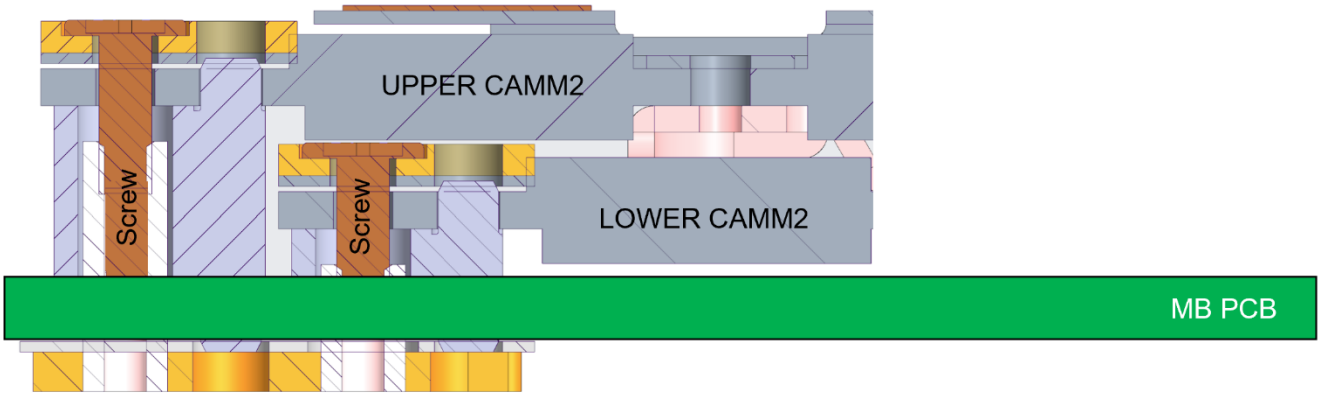
Not shown, an LP5 CAMM2 cannot mount because the "L" mounting holes do not align with the MB. This is intentional as DDR5 CAMM2 MBs do not support LP5 modules.

If a bottom bolster plate is implemented for use with screws to compress CAMM2's, its standoffs must be low-profile, so they do not protrude through the top surface of the MB PCB. If they do protrude, they may interfere with the body of CAMM2 Variation AXXX connector.



6.14 Informative: CAMM2 Mounting (cont'd)

A side view of stacked SC CAMM2's is shown here to depict how the mounting screws might work. Remember that the alignment posts provide tight X,Y alignment, while the screws provide compression in the Z axis.



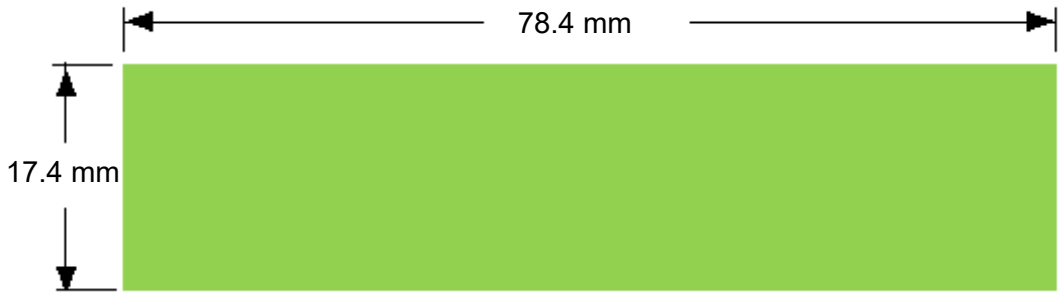
Other methods that do not use screws are allowed, and these methods are system-dependent and beyond the scope of this standard. System designs must assure sufficient compression is achieved while relying on the alignment posts for X,Y positioning.

6.15 CAMM2 PCB Layout Considerations

PCB layouts of modules must be compatible with all possible CAMM2 connectors and optimized for signal integrity. MBs are recommended to follow these layout considerations also.

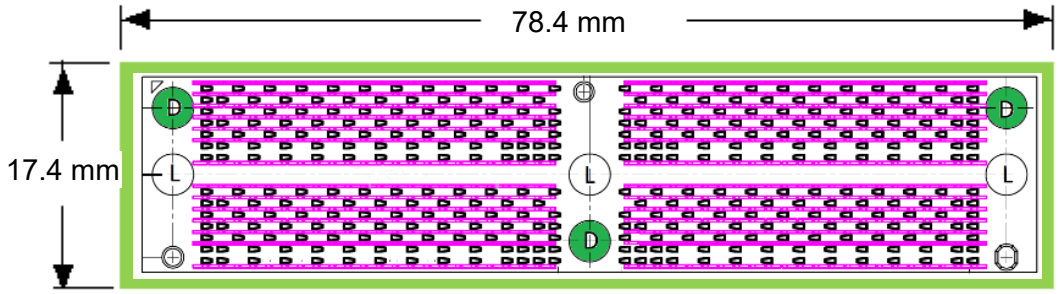
6.15.1 CAMM2 Ground Plane

Connector variations AXXX, BXXX, CXXX, DXXX are sized to mount on the same size PCB footprint, with exception of mounting holes described in paragraph 6.14. The connector body is 17 x 78 mm (two of BXXX use this same area). A solid ENIG-plated ground plane covers this area with exception of defined vias, pin pads, mounting holes, and alignment pins. In addition, the ground plane size should be extended by 0.2 mm to match the soldermask keepout as described next. The total ground plane area is recommended to be 17.4 x 78.4 mm.



6.15.1 CAMM2 Ground Plane (cont'd)

When the connector is seated on the ground plane, there should be a 0.2 mm typical spacing around the periphery of the connector. This spacing allows for all tolerances and any imperfections in soldermask that surrounds this plane.



Trace routing should not be allowed within the ground plane area.

- For connectors with embedded ground shields (e.g. variations AXXX and BXXX), the length of each ground shield segment is variable by supplier. For example, one supplier may have a ground shield that covers 5 ground pad locations while another supplier may have a ground shield that covers 6 ground pad locations. This means the break in between ground shield segments is not specified, so any trace routing within the ground plane may inadvertently align with these breaks between ground shield segments which could lead to a subtle signal integrity weakness. Ground shields may be shaped like below where the top and bottom contacts connect to the MB and module ground planes respectively:

- Traces within the ground plane would be ENIG-plated and soldermask is not allowed (see paragraph 6.15.2), so dielectric constants will be different in this region.
- Traces within the ground plane may short to ground shield locations. For example, a layout that is intended to be used with connector variation CXXX or DXXX (which have no ground shields) may have no issue with traces within the ground plane, however when connector variation AXXX is used for test purposes or to raise the CAMM2 higher into air flow, then the ground shields of connector AXXX may short to said traces.
- Future versions of the CAMM2 connector may require additional grounding to achieve considerably faster speeds. While the DXXX variation today has no ground shields, the availability of the full ground plane offers future flexibility for addition of ground shields within the connector.

Ground planes are required for all CAMM2 modules and recommended for all motherboards. This provides compatibility across modules and connectors. For example, while a combination of MB + connector DXXX + LP5 CAMM2 is common, the combination of MB + connector AXXX + LP5 CAMM2 is also valid. This latter case may be used when the system designer needs the module higher from the MB for better air flow or placement of components under the module.

6.15.1 CAMM2 Ground Plane (cont'd)

In another example, while the combination of MB + connector AXXX + DDR5 CAMM2 is common, the combination of MB + connector CXXX + DDR5 CAMM2 is also valid. This case may be used when the system designer cantilevers the module off the MB edge and desires a lower height profile of a 1.0mm CXXX connector.

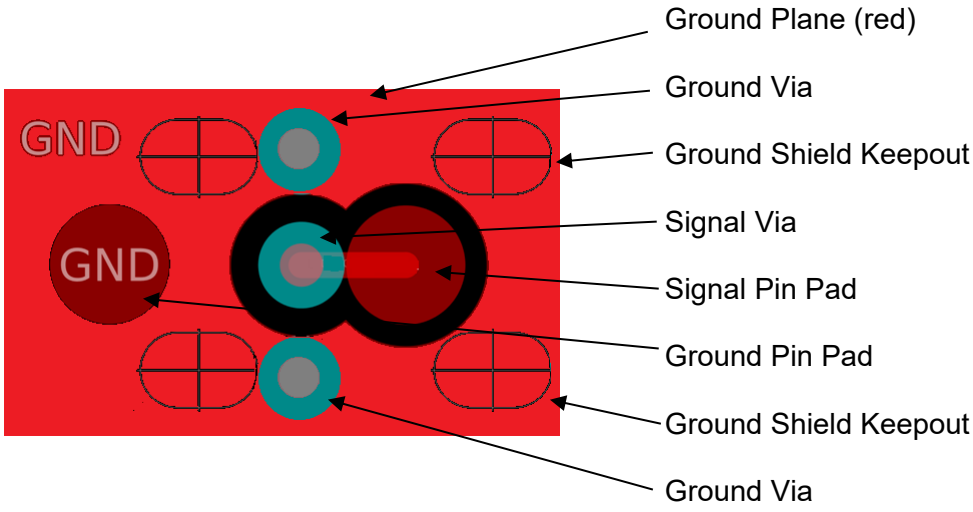
6.15.2 CAMM2 Soldermask Keepout

Soldermask keepout is required for all CAMM2 modules and recommended for all motherboards. The CAMM2 connector must sit flat on the ground plane to assure consistent contact force. Any soldermask between the connector and ground plane will block the connector body from fully seating as intended, which detracts from the contact travel, force and resistance.

6.15.3 Recommended Via Patterns

The pad and via arrangement should consider these factors:

- Ground vias close to signal vias are important for signal return current.
- Vias cannot reside inside a pad because the CAMM2 contact needs a reliable flat mating surface
- Ground shield keepout (oval areas below) are fully incorporated within the ground plane. This keepout is shown to depict the landing zone for ground shields within some CAMM2 connectors. These keepouts are not separate pads.
- Zero spacing between the signal pad and signal via (blue pad adjacent to red pad) is ok since there is no need for a solder paste dam. Solder paste and solder mask are not allowed in the CAMM2 region.



6.15.3 Recommended Via Patterns (cont'd)

Via size = 16R8

- Drill size = 8 mil (0.2032 mm)
- Pad size = 16 mil (0.4064 mm)
- Anti-pad size = 26 mil (0.6604 mm)

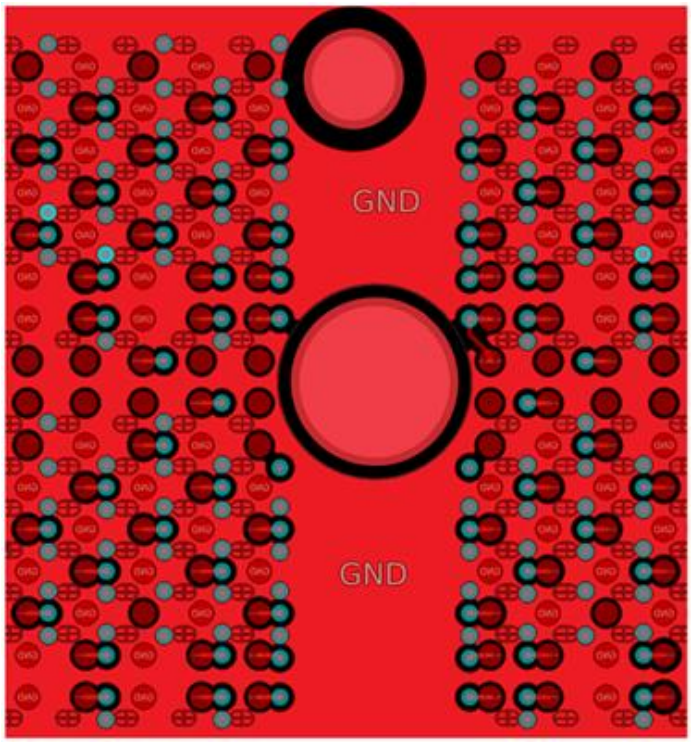
Signal pad size = 22 mil (0.5600 mm)
Signal pad anti-pad = 32mil (0.8128 mm)

Ground shield keepout oval =
13.77 x 21.65 mils
(0.35 x 0.55 mm)

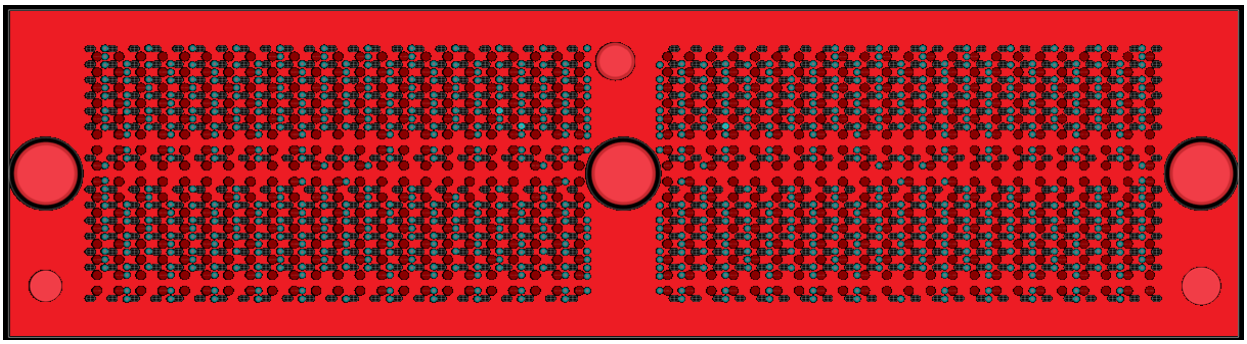
Larger via size, like 18R8, is also possible with this pad/via pattern.

Micro vias in HDI designs are also possible but should not reside in pads. If in-pad vias are necessary, thicker ENIG plating is recommended to assure a flat contact surface.

When the above pattern is scaled out for the full connector, the pattern looks like this:



The recommended via/pad array for the full connector is shown below (with LP5 CAMM2 mounting holes). Note vias for the center two rows are missing since many pads are RFU. Future vias for these locations would follow the same placement pattern as above.



7 CAMM2 Impedance Profile

CAMM2 impedance Profile is documented in each Annex.

8 Serial Presence Detect Component Specification

Please refer to the latest version of JESD400-5: DDR5 Serial Presence Detect (SPD) Contents.
Please refer to the latest version of JESD406-5: LPDDR5/5X Serial Presence Detect (SPD) Contents

9 Product Label

Please refer to the latest version of JESD401-5: DDR5 DIMM Label.

10 JEDEC Process

JEDEC provides PCB reference designs for modules. The designs are divided into families, one of which is Compression-Attached Memory Modules (CAMM2s). Letters (A, B, C, etc.) are used to define specific configurations (raw cards) of modules such as 2 ranks with x8 based SDRAMs. Additional characteristics may further refine cards into specific raw card (R/C) letters. Letter assignments are arbitrary and usually chronological. There is no other association to the letter assignments.

R/Cs are reviewed and balloted by JEDEC members before being placed on the JEDEC website as reference designs. This is called registration. The initial registration is 0. A specific card may be the registration of R/C A0. Subsequent design updates to the reference design go through the same balloting process and increment the registration number from 0 to 1 or the next highest number.

Annex A — (Informative) Difference between JESD318A and JESD318

This annex briefly describes most of the changes made to entries that appear in this standard, JESD318A (December 2024), compared to its predecessor, JESD318 (November 2023)

- Modified DDR5 length matching rules per TG consensus
- Changed “diff” to “differential” throughout the document
- Paragraph 5.2, Modified decoupling to match LP5 CAMM2 design
- Paragraph 5.3, Added TVS requirement
- Paragraph 6.13, Clarified rules apple to both DDR5 and LP5 CAMM2s
- Updated revision number to avoid confusion with other releases
- Added optional pins: VDDQ, VDDQ_DISABLE
- Added Paragraph 4.3 VDDQ Power Delivery Methods
- Added GSI_n pin to LP5 CAMM2 pinout
- Three “DDR6 RFU” pins changed to optional “RFU” in anticipation of a revised connector with additional pins
- Corrected Table 20 lengths.
- Replaced “LPDDR5/5X” with “LP5” per TG suggestion to simplify language
- Moved VDDQ and RFU pin assignments for LP5 CAMM2 pinout
- Paragraph 6.14 added as an informative section

Annex B — (Informative) Difference between JESD318B and JESD318A

This annex briefly describes most of the changes made to entries that appear in this standard, JESD318B (November 2025), compared to its predecessor, JESD318A (December 2024)

Rev 1.13 changes:

- GND_Detect_n pin added for use on LP5 CAMM2
- Table 12 updated for voltage levels and frequency range
- Paragraph 6.15 added as an informative section
- Paragraph 3.7 Corrected DQS signal definition to match LPDDR5 DRAM definition
- Paragraph 3.2 and 3.7 Corrected IO Levels from VDD to VDDQ for several signals

Rev 1.14 changes:

- Paragraph 4.2 Changed Soft Stop Time from 4ms to 8ms to match PMIC spec
- Paragraph 6.10.10 Changed title from CA to CAI
- Paragraph 8. Added LPDDR5 SPD reference
- Table 23. Fixed typo of 0.0100 to 0.100 and removed items 28-30 as these were carryovers from DIMM rules

Standard Improvement Form **JEDEC Standard** **JESD318B**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

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3. Other suggestions for document improvement:

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